# PCM-3810I

**PCI-104 12-bit Multifunction Module**

# User Manual

**Acknowledgements**

Intel and Pentium are trademarks of Intel Corporation.

Microsoft Windows and MS-DOS are registered trademarks of

Microsoft Corp.

All other product names or trademarks are properties of their respective owners.

Part No. 2003381000 1st Edition

Printed in Taiwan December 2009

**Product Warranty (2 years)**

Advantech warrants to you, the original purchaser, that each of its products will be free from defects in materials and workmanship for two years from the date of purchase.

This warranty does not apply to any products which have been repaired or altered by persons other than repair personnel authorized by Advantech, or which have been subject to misuse, abuse, accident or improper installation. Advantech assumes no liability under the terms of this warranty as a consequence of such events.

Because of Advantech's high quality-control standards and rigorous testing, most of our customers never need to use our repair service. If an Advantech product is defective, it will be repaired or replaced at no charge during the warranty period. For out-of-warranty repairs, you will be billed according to the cost of replacement materials, service time and freight. Please consult your dealer for more details.

If you think you have a defective product, follow these steps:

1. Collect all the information about the problem encountered. (For example, CPU speed, Advantech products used, other hardware and software used, etc.) Note anything abnormal and list any onscreen messages you get when the problem occurs.
2. Call your dealer and describe the problem. Please have your manual, product, and any helpful information readily available.
3. If your product is diagnosed as defective, obtain an RMA (return merchandize authorization) number from your dealer. This allows us to process your return more quickly.
4. Carefully pack the defective product, a fully-completed Repair and Replacement Order Card and a photocopy proof of purchase date (such as your sales receipt) in a shippable container. A product returned without proof of the purchase date is not eligible for warranty service.
5. Write the RMA number visibly on the outside of the package and ship it prepaid to your dealer.

**CE**

This product has passed the CE test for environmental specifications when shielded cables are used for external wiring. We recommend the use of shielded cables. This kind of cable is available from Advantech. Please contact your local supplier for ordering information.

**Technical Support and Assistance**

Step 1. Visit the Advantech web site at **www.advantech.com/support** where you can find the latest information about the product.

Step 2. Contact your distributor, sales representative, or Advantech's customer service center for technical support if you need additional assistance. Please have the following information ready before you call:
- Product name and serial number
- Description of your peripheral attachments
- Description of your software (operating system, version, application software, etc.)
- A complete description of the problem
- The exact wording of any error messages

**Packing List**

Before setting up the system, check that the items listed below are included and in good condition. If any item does not accord with the table, please contact your dealer immediately.

- PCM-3810I DA&C card
- PCM-3810I User Manual
- Companion CD-ROM with DLL drivers

**Safety Precaution - Static Electricity**

Follow these simple precautions to protect yourself from harm and the products from damage.

1. To avoid electrical shock, always disconnect the power from your PC chassis before you work on it. Don't touch any components on the CPU card or other cards while the PC is on.
2. Disconnect power before making any configuration changes. The sudden rush of power as you connect a jumper or install a card may damage sensitive electronic components.

# Contents

CHAPTER 1

# Introduction

This chapter introduces the PCM-3810I card and its typical applications.

Sections include:

- Features
- Applications
- Installation Guide
- Software Overview
- Device Driver Roadmap
- Accessories

# Chapter 1 Introduction

The PCM-3810I is a PCI-104 multifunction card for IBM PC/XT/AT or compatible computers. It offers the five most desired measurement and control functions:

- 12-bit A/D conversion
- 12-bit D/A conversion
- Digital input
- Digital output
- Timer/counter.

A programmable-gain instrument amplifier lets you acquire different input signals without external signal conditioning. An onboard 4k word FIFO buffer provides high-speed data transfer and predictable performance under Windows. Automatic channel scanning circuitry and onboard SRAM let you perform multiple-channel A/D conversion and individual gains for each channel.

The following sections of this chapter will provide further information about features of the multifunction cards, a Quick Start for installation, together with some brief information on software and accessories for the PCM-3810I cards.

## 1.1 Features

- 16 single-ended or 8 differential A/D inputs, programmable
- 12-bit A/D converter, up to 250 kHz sampling rate
- Instantly software polling, 1 μs high-speed response
- Double-Clock acquisition operation for analog input
- Pre-, Post-, About-, and Delay- event trigger capable
- Programmable gain for each input channel, automatic channel/gain scanning
- 4K onboard ring buffer for analog input and output
- Two independent 12-bit analog output channels with continuous waveform output function of maximum 250KHz throughput rate
- Auto-Calibration for analog input and output channels
- 16 digital Input and output channels, TTL compatible
- Three 24-bit independent full function counters
- BoardID switch

PCM-3810I offers the following main features:

**PCI-Bus Plug & Play**

The PCM-3810I card uses a PCI controller to interface the card to the PCI-104 bus. The controller fully implements the PCI bus specification Rev 2.2. All configurations related to the bus, such as base address and interrupt assignment, are automatically controlled by software. No jumper or switch is required for user configuration.

**Automatic Channel/Gain Scanning**

PCM-3810I features an automatic channel/gain scanning circuit. This circuit, instead of your software, controls multiplexer switching during sampling. On-board SRAM stores different gain values for each channel. This combination lets user perform multi-channel high-speed sampling (up to 250 kHz) for each channel.

**Onboard Ring Buffer Memory**

There are 4k samples ring buffer for A/D and D/A on PCM-3810I. This is an important feature for faster data transfer and more predictable performance under Windows system.

**Onboard Programmable Timer/Counter**

PCM-3810I features three 24-bit timer/counters to provide one shot output, PWM output, periodic interrupt output, time-delay output, and the measurement of frequency and pulse width.

**BoardID Switch**

PCM-3810I has a built-in DIP switch that helps define each card's ID when multiple PCM-3810I cards have been installed on the same PC chassis. The BoardID setting function is very useful when building a system with multiple PCM-3810I cards. With the correct BoardID settings, you can easily identify and access each card during hardware configuration and software programming.

*Note: For detailed specifications and operation theory of the PCM-3810I, please refer to Appendix A and B.*

## 1.2 Applications

- Transducer and sensor measurements
- Waveform acquisition and analysis
- Process control and monitoring
- Vibration and transient analysis

## 1.3 Installation Guide

Before you install your PCM-3810I card, please make sure you have the following necessary components:

- PCM-3810I DA&C card
- PCM-3810I User Manual
- Driver software Advantech DLL drivers (included in the companion CD-ROM)
- Personal computer or workstation with a PCI-104 interface (running Windows 2000/XP/Vista)
- 50-pin/26-pin Flat Cable (optional)
- Wiring board (optional)

Other optional components are also available for enhanced operation:

- A-DAQ Pro, LabView or other 3rd-party software

After you get the necessary components and maybe some of the accessories for enhanced operation of your multifunction card, you can then begin the installation procedure. Figure 1.1 on the next page provides a concise flow chart to give users a broad picture of the software and hardware installation procedures:

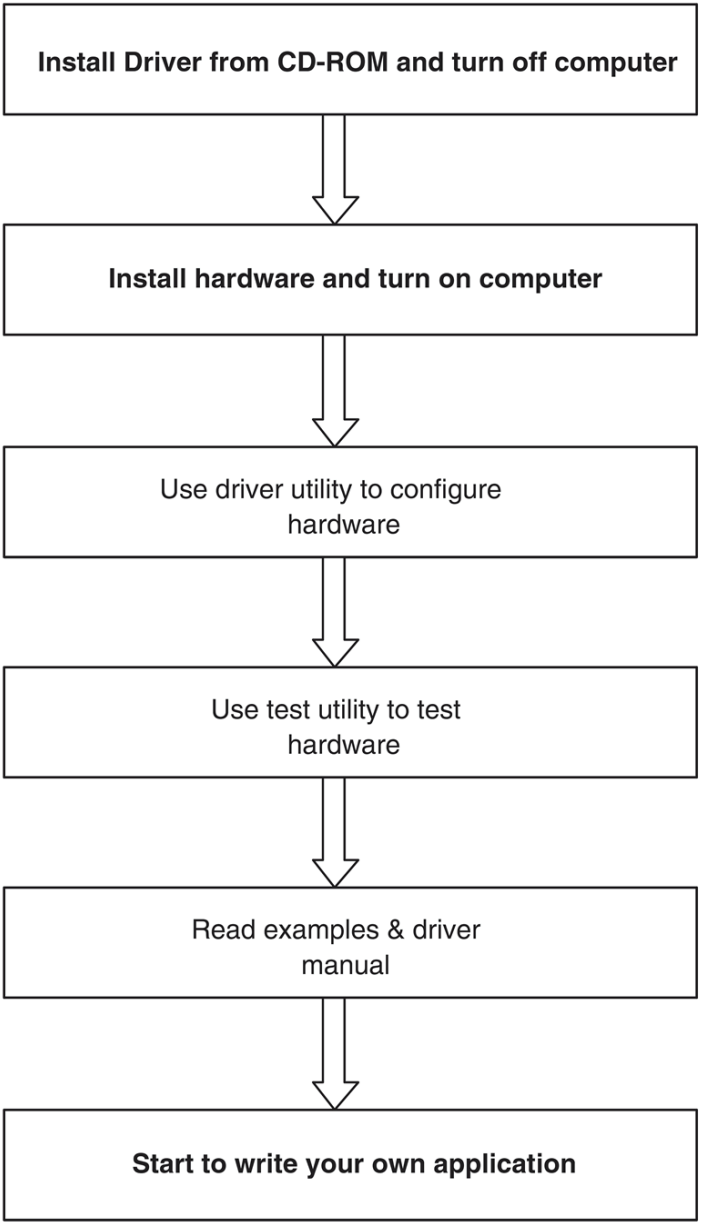



***Figure 1.1: Installation Flow Chart***

## 1.4 Software Overview

Advantech offers a rich set of DLL drivers, third-party driver support and application software to help fully exploit the functions of your PCM-3810I card:

- Device Drivers (on the companion CD-ROM)
- LabVIEW driver
- Advantech A-DAQ Pro
- WaveScan

**Programming choices for DA&C cards**

You may use Advantech application software such as Advantech Device Drivers. On the other hand, advanced users can use register-level programming, although this is not recommended due to its laborious and time-consuming nature.

**Device Drivers**

Advantech Device Driver software is included on the companion CD-ROM at no extra charge. It also comes with all Advantech DA&C cards. Advantech's Device Drivers features a complete I/O function library to help boost your application performance. Advantech Device Drivers for Windows 2000/XP/Vista works seamlessly with development tools such as Visual Studio .Net, Visual C++, Visual Basic, Borland C++ Builder and Borland Delphi.

## 1.5 Device Driver Programming Roadmap

This section will provide you a roadmap to demonstrate how to build an application from scratch using Advantech Device Drivers with your favorite development tools such as Visual Studio .Net, Visual C++, Visual Basic, Delphi and C++ Builder. The step-by-step instructions on how to build your own applications using each development tool will be given in the *Device Drivers Manual*. Moreover, a rich set of example source code is also given for your reference.

**Programming Tools**

Programmers can develop application programs with their favorite development tools:

- Visual Studio .Net
- Visual C++ and Visual Basic
- Delphi
- C++ Builder

For instructions on how to begin programming works in each development tool, Advantech offers a *Tutorial* Chapter in the *Device Drivers Manual* for your reference. Please refer to the corresponding sections in this chapter on the *Device Drivers Manual* to begin your programming efforts. You can also look at the example source code provided for each programming tool, since they can get you very well oriented.

The *Device Drivers Manual* can be found on the companion CD-ROM. Alternatively, if you have already installed the Device Drivers on your system, The *Device Drivers Manual* can be readily accessed through the Start button:

***Start/Programs/Advantech Automation/Device Manager/ Device Drivers Manual***

The example source code could be found under the corresponding installation folder such as the default installation path:

***\Program Files\Advantech\ADSAPI\Examples***

For information about using other function groups or other development tools, please refer to the *Creating Windows 2000/XP/Vista Application with Device Drivers* chapter and the *Function Overview* chapter on the *Device Drivers Manual*.

**Programming with Device Drivers Function Library**

Advantech Device Drivers offer a rich function library that can be utilized in various application programs. This function library consists of numerous APIs that support many development tools, such as Visual Studio .Net, Visual C++, Visual Basic, Delphi and C++ Builder.

According to their specific functions or services, APIs can be categorized into several function groups:

- Analog Input Function Group
- Analog Output Function Group
- Digital Input/Output Function Group
- Counter Function Group
- Port Function Group (direct I/O)
- Event Function Group

For the usage and parameters of each function, please refer to the *Function Overview* chapter in the *Device Drivers Manual*.

**Troubleshooting Device Drivers Error**

Driver functions will return a status code when they are called to perform a certain task for the application. When a function returns a code that is not zero, it means the function has failed to perform its designated function. To troubleshoot the Device Drivers error, you can pass the error code to DRV_GetErrorMessage function to return the error message. Alternatively, you can refer to the *Device Drivers Error Codes* Appendix in the *Device Drivers Manual* for a detailed listing of Error Codes, Error IDs and Error Messages.

## 1.6 Accessories

Advantech offers a complete set of accessory products to support the PCM-3810I card. These accessories include:

**Wiring Cables**

- PCL-10150 IDC-50 Flat Cable
- PCL-10126 IDC-26 to DB-25 Cable

**Wiring Boards**

- **ADAM-3950** 50-pin Flat Cable Wiring Terminal
- **ADAM-3925** DB-25 Wiring Terminal

CHAPTER 2

# Installation

This chapter provides a packaged item checklist, proper instructions for unpacking and step-by-step procedures for both driver and card installation..

Sections include:

- Unpacking
- Driver Installation
- Hardware Installation
- Device Setup & Configuration

# Chapter 2 Installation

## 2.1 Unpacking

After receiving your PCM-3810I package, please inspect its contents first. The package should contain the following items:

- PCM-3810I card
- Companion CD-ROM (Device Drivers included)
- User Manual

The PCM-3810I card harbor certain electronic components vulnerable to *electrostatic discharge* (ESD). ESD can easily damage the integrated circuits and certain components if preventive measures are ignored.

Before removing the card from the antistatic plastic bag, you should take the following precautions to ward off possible ESD damage:

- Touch the metal part of your computer chassis with your hand to discharge the static electricity accumulated on your body. Alternatively, one can also use a grounding strap.
- Touch the anti-static bag to a metal part of your computer chassis before opening the bag.
- Take hold of the card only by the metal bracket when removing it out of the bag.

After taking out the card, you should first:

- Inspect the card for any possible signs of external damage (loose or damaged components, etc.). If the card is visibly damaged, please notify our service department or our local sales representative immediately. Do not install a damaged card into your system.

Also, pay extra caution to the following aspects during installation:

- Avoid physical contact with materials that could hold static electricity such as plastic, vinyl and Styrofoam.
- Whenever you handle the card, grasp it only by its edges. DO NOT TOUCH the exposed metal pins of the connector or the electronic components.

.

*Note:* *Keep the anti-static bag for future use. You might need the original bag to store the card if you have to remove the card from a PC or transport it elsewhere.*

## 2.2 Driver Installation

We recommend you install the driver before you install the PCM-3810I card into your system, since this will guarantee a smooth installation process.

The Advantech Device Drivers Setup program for the PCM-3810I card is included in the companion CD-ROM that is shipped with your DA&C card package. Please follow the steps below to install the driver software:

1. Insert the companion CD-ROM into your CD-ROM drive.
2. The Setup program will be launched automatically if you have the autoplay function enabled on your system. When the Setup Program is launched, you will see the following Setup Screen.

*Note:* *If the autoplay function is not enabled on your computer, use Windows Explorer or Windows Run command to execute autorun.exe on the companion CD-ROM.*

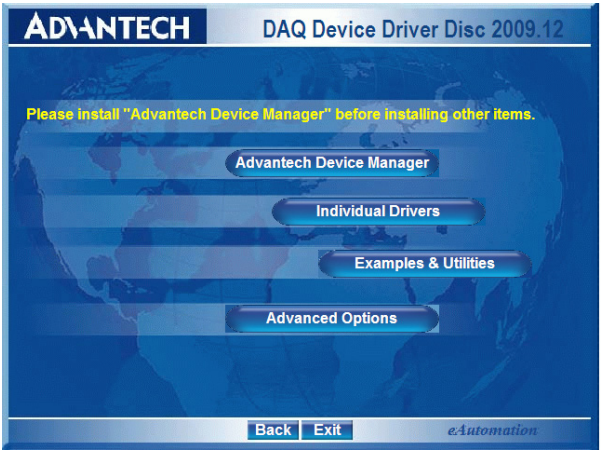



***Figure 2.1: Setup Screen of Advantech Automation Software***

3. Select the Device Manager option to install.
4. Select the *Individual Driver* option.
5. Select the specific device then follow the installation instructions step by step to complete your device driver installation and setup.

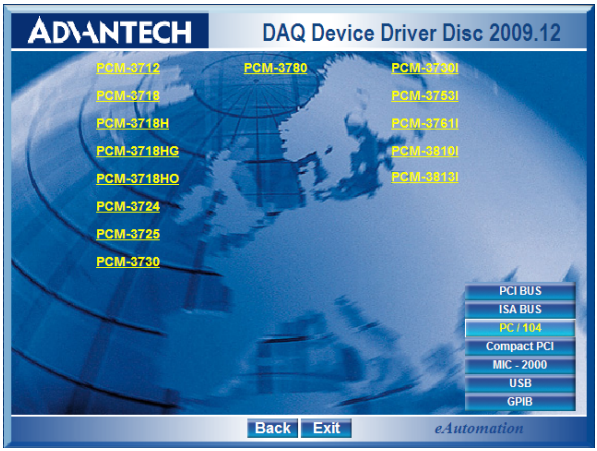



***Figure 2.2: Different Options for Driver Setup***

For further information on driver-related issues, an online version of the *Device Drivers Manual* is available by accessing the following path:

*Start/Programs/Advantech Automation/Device Manager/Device Drivers Manual*

## 2.3 Hardware Installation

*Note:* *Make sure you have installed the driver before you install the card (please refer to chapter 2.2 Driver Installation)*

After the Device Drivers installation is completed you can install the PCM-3810I card on your computer. However, it is suggested that you refer to the computer's user manual or related documentation if you have any doubts. Please follow the steps below to install the card onto your system.

1. Turn off your computer and unplug the power cord and cables. TURN OFF your computer before installing or removing any components on the computer.
2. Remove the cover of your computer.
3. Remove the slot cover on the back panel of your computer.
4. Touch the metal part on the surface of your computer to neutralize the static electricity that might be on your body.
5. Insert the PCM-3810I card into the PCI-104 interface. Hold the card only by its edges and carefully align it with the slot. Insert the card firmly into place. Use of excessive force must be avoided; otherwise, the card might be damaged.
6. Connect appropriate accessories (50-pin cable, wiring terminals, etc. if necessary) to the card.
7. Replace the cover of your computer chassis. Re-connect the cables you removed in step 2.
8. Plug in the power cord and turn on the computer.

After your card is properly installed on your system, you can now configure your device using the *Advantech Device Manager* Program that has itself already been installed on your system during driver setup. A complete device installation procedure should include *device setup*, *configuration* and *testing*. The following sections will guide you through the Setup, Configuration and Testing of your device.

## 2.4 Device Setup & Configuration

The *Advantech Device Manager* program is a utility that allows you to set up, configure and test your device, and later stores your settings on the system registry. These settings will be used when you call the APIs of Advantech Device Drivers.

**Setting Up the Device**

1. To install the I/O device for your card, you must first run the *Device Manager* program (by accessing *Start/Programs/Advantech Automation/Device Manager/Advantech Device Manager* ).
2. You can then view the device(s) already installed on your system (if any) on the *Installed Devices* list box. If the software and hardware installation are completed, you will see PCM-3810I card in the Installed Devices list.

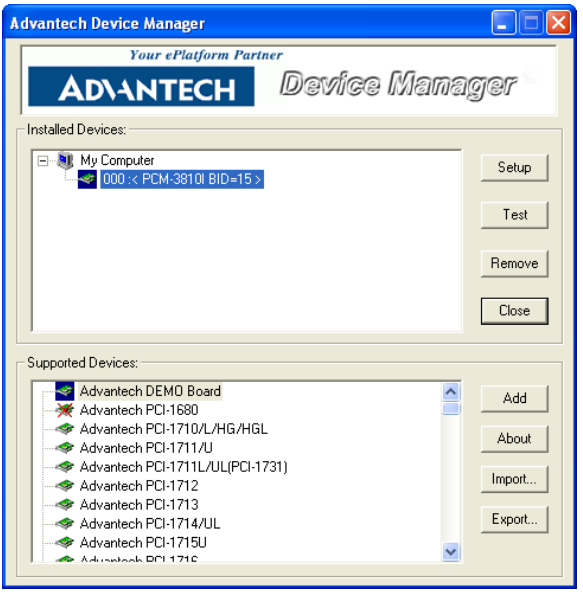



***Figure 2.3: The Device Manager Dialog Box***

**Configuring the Device**

3. Please click the Setup button to configure your device. On the *Device Setting* dialog box (Fig. 2-4), you can configure the Analog Input (Fig. 2-5), Analog Output (Fig. 2-6) and Digital Input/Output (Fig. 2-7) of PCM-3810I.

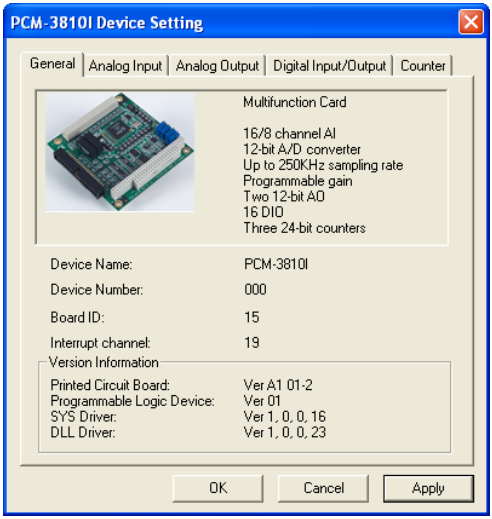



***Figure 2.4: The Device Setting Dialog Box***

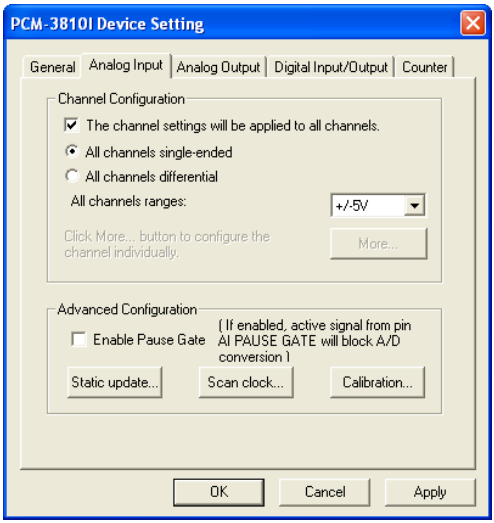



***Figure 2.5: Analog Input Configuration***

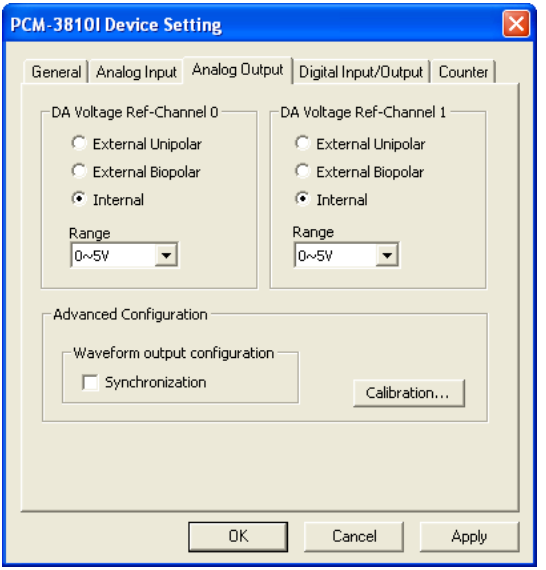



***Figure 2.6: Analog Output Configuration***

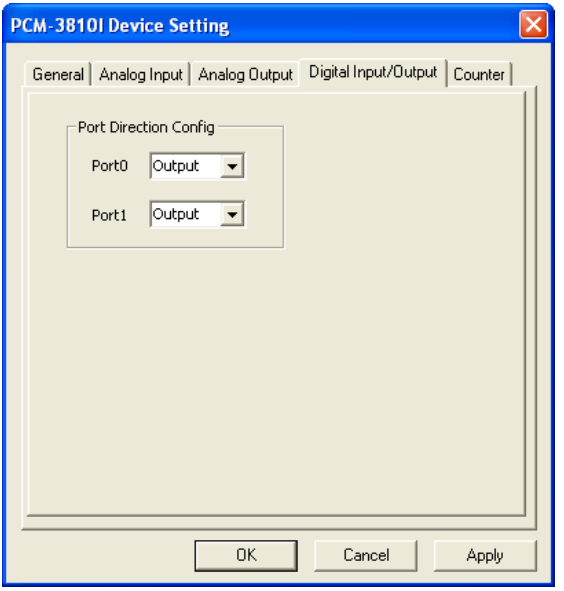



***Figure 2.7: Digital Input/Output Configuration***

4. After your card is properly installed and configured, you can click the *Test...* button to test your hardware by using the testing utility supplied.

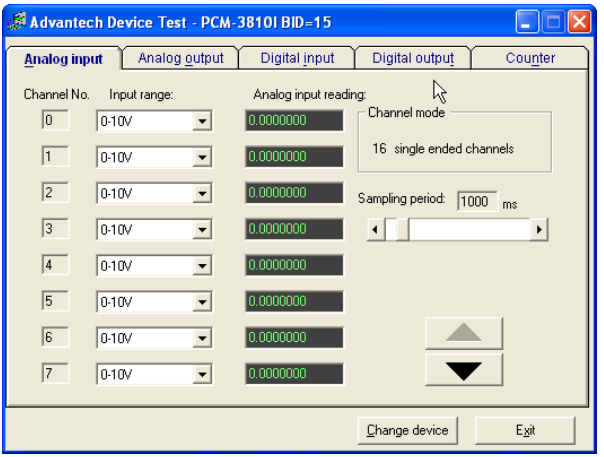



***Figure 2.8: The Test Utility Dialog Box***

For more detailed information, please refer to *Chapter 2* of the *Device Drivers Manual*. You can also find rich examples on the CD-ROM to speed up your programming.

CHAPTER 3

# Signal Connections

This chapter provides useful information about how to connect input and output signals to the PCM-3810I card via the I/O connector.

Sections include:

- Overview
- BoardID Settings
- Signal Connections
- Field Wiring Considerations

# Chapter 3 Signal Connections

## 3.1 Overview

Maintaining signal connections is one of the most important factors in ensuring that your application system is sending and receiving data correctly. A good signal connection can avoid unnecessary and costly damage to your PC and other hardware devices. This chapter provides useful information about how to connect input and output signals to the PCM-3810I card via the I/O connector.

## 3.2 Switch and Jumper Settings

The following figure will show you the locations for switches and connectors for PCM-3810I.

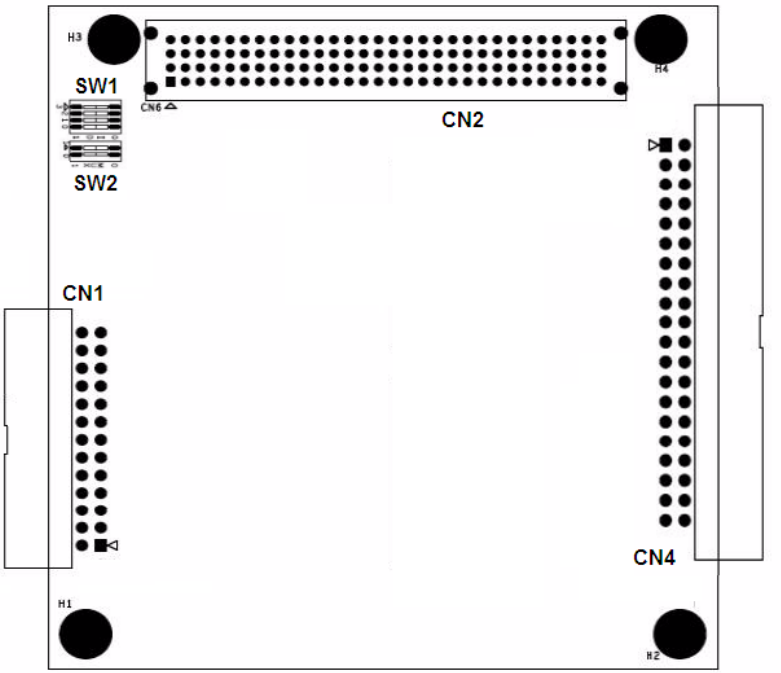



***Figure 3.1: Connector and Switch Locations***

BoardID settings are used to set a board's unique identifier when multiple identical cards are installed in the same system.

PCM-3810I card has a built-in DIP switch (SW1), which is used to define each card's unique identifier. You can determine the unique identifier in the register as shown in Table 3.1. If there are multiple identical cards in the same chassis, the BoardID switch helps differentiate the boards by identifying each card's device number with the switch setting. The BoardID switch's unique identifier has been set to 0 at the factory.

If you need to adjust it to other numbers, set SW1 by referring to DIP switch settings below.

*Table 3.1: Board ID Setting (SW1)*

| SW1 | Position 1 | Position 2 | Position 3 | Position 4 |
|---|---|---|---|---|
| **BoardID** | **ID3** | **ID2** | **ID1** | **ID0** |
| **0** | ON | ON | ON | ON |
| **1** | ON | ON | ON | OFF |
| **2** | ON | ON | OFF | ON |
| **3** | ON | ON | OFF | OFF |
| **4** | ON | OFF | ON | ON |
| **5** | ON | OFF | ON | OFF |
| **6** | ON | OFF | OFF | ON |
| **7** | ON | OFF | OFF | OFF |
| **8** | OFF | ON | ON | ON |
| **9** | OFF | ON | ON | OFF |
| **10** | OFF | ON | OFF | ON |
| **11** | OFF | ON | OFF | OFF |
| **12** | OFF | OFF | ON | ON |
| **13** | OFF | OFF | ON | OFF |
| **14** | OFF | OFF | OFF | ON |
| **15** | OFF | OFF | OFF | OFF |

Default Setting is 0

### 3.2.1 CLK and INT Setting (SW2)

If multiple PCM-3810I cards are installed in the system, different CLK and INT signals must be set. SW2 is used for the setting of IDSEL, CLK and INT. One system can support up to 4 PCM-3810I cards.

*Table 3.2: CLK and INT Setting*

| Position 1 | Position 2 | CLK | INT # |
|---|---|---|---|
| ON | ON | CLK0 | INT A# |
| ON | OFF | CLK1 | INT B# |
| OFF | ON | CLK2 | INT C# |
| OFF | OFF | CLK3 | INT D# |

## 3.3 Signal Connections

**Pin Assignments**

There are two I/O connectors on the PCM-3810I. Figure 3-2 and Figure 3-3 show the ping assignments for the 50-pin I/O connector (CN4) and the 26-pin I/O connector (CN3).

| | | | |
|---|---|---|---|
| AI DIG TRIG | 1 | 2 | DGND |
| AI PAUSE GATE | 3 | 4 | DGND |
| AI SCAN CLK | 5 | 6 | DGND |
| AI CONV CLK | 7 | 8 | DGND |
| AO START TRIG | 9 | 10 | DGND |
| AO CONV CLK | 11 | 12 | DGND |
| NC | 13 | 14 | DGND |
| CNT0 CLK | 15 | 16 | CNT0 GATE |
| CNT0 OUT | 17 | 18 | DGND |
| CNT1 CLK | 19 | 20 | CNT1 GATE |
| CNT1 OUT | 21 | 22 | DGND |
| CNT2 CLK | 23 | 24 | CNT2 GATE |
| CNT2 OUT | 25 | 26 | DGND |
| DGND | 27 | 28 | DGND |
| DIO0 | 29 | 30 | DIO1 |
| DIO2 | 31 | 32 | DIO3 |
| DIO4 | 33 | 34 | DIO5 |
| DIO6 | 35 | 36 | DIO7 |
| DGND | 37 | 38 | DGND |
| DIO8 | 39 | 40 | DIO9 |
| DIO10 | 41 | 42 | DIO11 |
| DIO12 | 43 | 44 | DIO13 |
| DIO14 | 45 | 46 | DIO15 |
| DGND | 47 | 48 | DGND |
| +5V | 49 | 50 | +12V |

***Figure 3.2: 50-pin I/O Connector Pin Assignments***

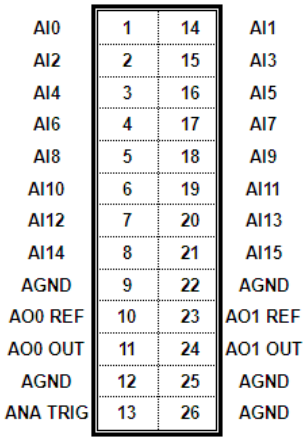



***Figure 3.3: 26-pin I/O Connector Pin Assignments***

If PCL-10126 is connected to the 26-pin I/O connector (CN3), the pin assignment for PCL-10126's DB-25 is shown in Figure 3-4.

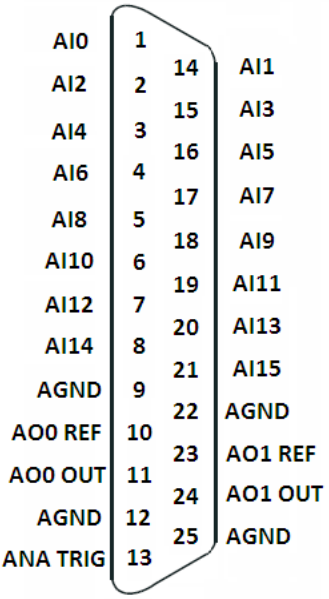



***Figure 3.4: PCL-10126 DB-25 I/O Connector Pin Assignments***

### 3.3.1 I/O Connector Signal Description

*Table 3.3: I/O Connector Signal Descriptions*

| Signal Name | Reference | Direction | Description |
|---|---|---|---|
| AI<0…15> | AGND | Input | **Analog Input Channels 0 to 15.** Each channel pair, AI<i, i+1> (i = 0, 2, 4...14), can be configured as either two single-ended inputs or one differential input. |
| AGND | - | - | **Analog Ground.** These pins are the reference points for single-ended measurements and the bias current return point for differential measurement. The ground references (AGND and DGND) are connected together on the PCM-3810I. |
| ANA TRIG | AGND | Input | **Analog threshold Trigger.** This pin is the analog input threshold trigger input. |
| AI DIG TRIG | DGND | Input | **Analog Input Digital Trigger.** This pin is used to execute a specific data acquisition mode - an acquisition which consists of one or more scans. |
| AI PAUSE GATE | DGND | Input | **Analog Input Pause GATE.** This pin is used to pause and resume a data acquisition. The *AI Conversion Clock* pauses while the *AI Pause Gate* signal is active and resumes when the signal is inactive. The active level of the pause gate could be programmed to be high or low. |
| AI SCAN CLK | DGND | Input | **Analog Input Scan Clock.** This pin is used to initiate a set of data acquisition. The card samples the AI signals of every channel in the scan list once for every *AI Scan Clock*. |
| AI CONV CLK | DGND | Input | **Analog Input Conversion Clock.** This pin is to initiate a single A/D conversion on a single channel. A Scan (controlled by the *AI Scan Clock*) consists of one or more conversions. |

| | | | |
|---|---|---|---|
| AO0 REF AO1_REF | AGND | Input | **Analog Output Channel 0/1 External Reference.** This is the external reference input for the analog output channel 0/1. |
| AO0_OUT AO1_OUT | AGND | Output | **Analog Output Channels 0/1.** This pin supplies the voltage output of analog output channel 0/1. |
| AO START TRIG | DGND | Input | **Analog Output Start Trigger.** This pin is to initiate a waveform generation. If you do not use triggers, you can begin a generation with a software command. |
| AO CONV CLK | DGND | Input | **Analog Output Convert Clock.** This pin is to initiate AO conversion. Each sample updates the outputs of all of the DACs. You can specify an internal or external source for AO Convert Clock. |
| DIO<0..15> | DGND | Input | **Digital Input/ Output Channel 0 to 15.** These pins are digital input/ output which could be configured as general purpose digital inputs or outputs. |
| DGND | - | - | **Digital Ground.** This pin supplies the reference for the digital channels at the I/O connector as well as the +5 V and +12 V DC supply. The ground references (AGND and DGND) are connected together on the PCM-3810I. |
| CNT0 CLK CNT1 CLK CNT2 CLK | DGND | Input | **Counter 0/1/2 External Clock Input.** The clock input of counters can be either external (up to 10 MHz) or internal (1 MHz), as set by software. |
| CNT0 OUT CNT1 OUT CNT2 OUT | DGND | Output | Counter 0/1/2 Output. |

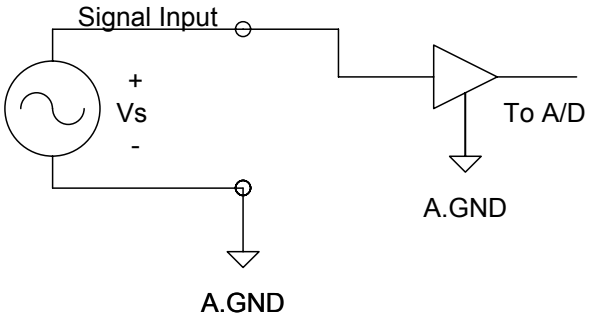
| | | | |
|---|---|---|---|
| CNT0 GATE<br>CNT1 GATE<br>CNT2 GATE | DGND | Input | Counter 0/1/2 Gate Control. |
| +12V | DGND | Output | **+12 VDC Source.** This pin is +12V DC power supply for external use. (1A maximum) |
| +5V | DGND | Output | **+5 VDC Source.** This pin is +5V DC power supply for external use. (1A maximum) |
| NC | - | - | **Not Connected.** These pins serve no connection. Do not connect signals to these pins for future compatibility. |

### 3.3.2 Analog Input Connections

PCM-3810I supports either 16 single-ended or 8 differential analog inputs.

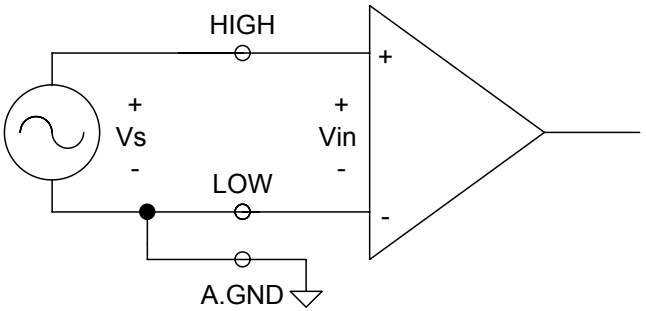
#### Single-ended Channel Connections

Single-ended connections use only one signal wire per channel. The voltage on the line references to the common ground on the card. A signal source without a local ground is called a "floating" source. It is fairly simple to connect a single ended channel to a floating signal source. A standard wiring diagram looks like this:



**Differential Channel Connections**

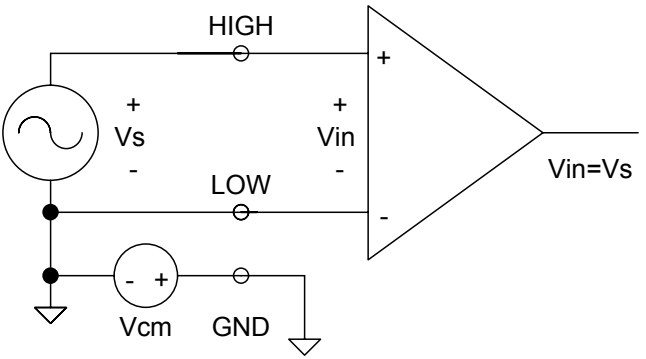
Differential input connections use two signal wires per channel. The card measures only the voltage difference between these two wires, the HIGH wire and the LOW wire. If the signal source has no connection to ground, it is called a "floating" source. A connection must exist between LOW and ground to define a common reference point for floating signal sources. To measure a floating sources connect the input channels as shown below:



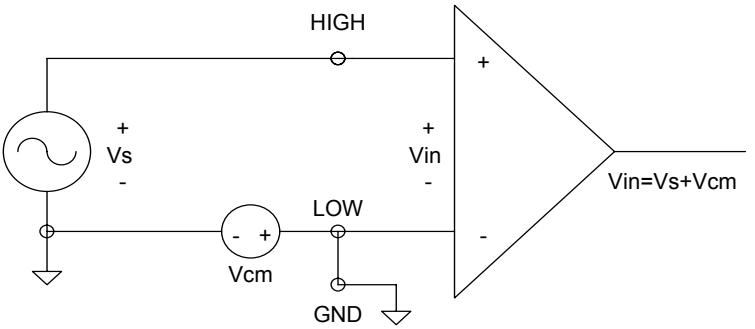

If the signal source has one side connected to a local ground, the signal source ground and the PCM-3810I ground will not be at exactly the same voltage, as they are connected through the ground return of the equipment and building wiring. The difference between the ground voltages forms a common-mode voltage.

To avoid the ground loop noise effect caused by common-mode voltages, connect the signal ground to the LOW input. Do not connect the LOW input to the PCM-3810I ground directly. In some cases you may also need a wire connection between the PCM-3810I ground and the signal source ground for better grounding. The following two diagrams show correct and incorrect connections for a differential input with local ground:

**Correct Connection**




**Incorrect Connection**




**Analog Output Connection**

The PCM-3810I provides two D/A output channels. You can use the internal precision -5 V or -10 V reference to generate 0 to +5 V or 0 to +10 V D/A output. Use an external reference for other D/A output ranges. The maximum reference input voltage is ±10 V and maximum output scaling is ±10 V. Loading current for D/A outputs should not exceed 5 mA.

Fig. 3-5 shows how to make analog output and external reference input connections on the PCM-3810I.

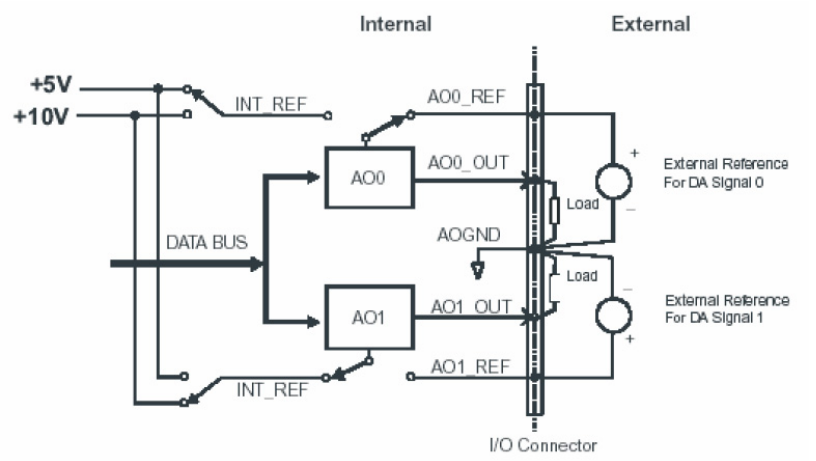
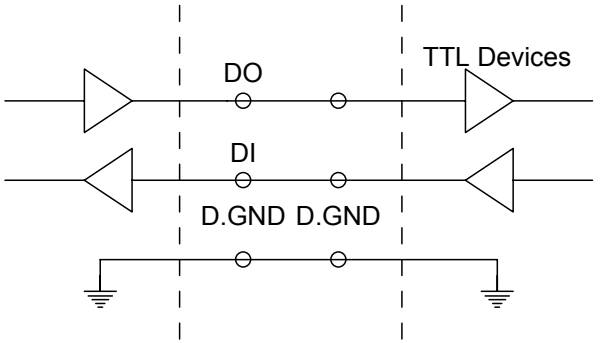



*Figure 3.5: Analog Output Connections*

### 3.3.3 Digital Signal Connections

The PCM-3810I has 16 digital input/output channels and they can be configured as input or output channels. The digital I/O levels are TTL compatible. The following figure shows connections to exchange digital signals with other TTL devices:



## 3.4 Field Wiring Considerations

When you use PCM-3810I cards to acquire data from outside, noises in the environment might significantly affect the accuracy of your measurements if due cautions are not taken. The following measures will be helpful to reduce possible interference running signal wires between signal sources and the PCM-3810I card.

- The signal cables must be kept away from strong electromagnetic sources such as power lines, large electric motors, circuit breakers or welding machines, since they may cause strong electromagnetic interference. Keep the analog signal cables away from any video monitor, since it can significantly affect a data acquisition system.
- If the cable travels through an area with significant electromagnetic interference, you should adopt individually shielded, twisted-pair wires as the analog input cable. This type of cable has its signal wires twisted together and shielded with a metal mesh. The metal mesh should only be connected to one point at the signal source ground.
- Avoid running the signal cables through any conduit that might have power lines in it.
- If you have to place your signal cable parallel to a power line that has a high voltage or high current running through it, try to keep a safe distance between them. Alternatively, you can place the signal cable at a right angle to the power line to minimize the undesirable effect.
- The signals transmitted on the cable will be directly affected by the quality of the cable. In order to ensure better signal quality, we recommend that you use the PCL-10150 and PCL-10126 cables.

APPENDIX A

# Specifications

# Appendix A Specifications

## A.1 Analog Input

| | | | | | | |
|---|---|---|---|---|---|---|
| **Channels** | 16 single-ended or 8 differential or combination | | | | | |
| **Resolution** | 12-bit | | | | | |
| **FIFO Size** | 4k samples | | | | | |
| **Max. Sampling Rate** | 250 kS/s | | | | | |
| **Input Range and Gain List** | Gain | 0.5 | 1 | 2 | 4 | 8 |
| | Unipolar | N/A | 0~10 | 0~5 | 0~2.5 | 0~1.25 |
| | Bipolar | ±10 | ±5 | ±2.5 | ±1.25 | ±0.625 |
| **Drift** | Gain | 0.5 | 1 | 2 | 4 | 8 |
| | Zero | 15 ppm/°C | | | | |
| | Span | 25 ppm/°C | | | | |
| **Small Signal BW for PGA** | Gain | 0.5 | 1 | 2 | 4 | 8 |
| | Bandwidth | 1MHz | 3.3MHz | 3.3MHz | 2.8MHz | 1.8MHz |
| **Max. Input Voltage** | ±15 V | | | | | |
| **Input Impedance** | 300 M ohm/ 5pF | | | | | |
| **Sampling Mode** | Software, on-board programmable pacer or external | | | | | |
| **Trigger Mode** | Pre-trigger, post-trigger, delay-trigger, about-trigger | | | | | |
| **Accuracy** | DC | INLE: ±1 LSB | | | | |
| | | DNLE: ±1 LSB | | | | |
| | | Offset error<1LSB | | | | |
| | | Gain | 0.5 | 1 | 2 | 4 | 8 |
| | | Gain Error (% FSR) | 0.1 | 0.1 | 0.2 | 0.2 | 0.4 |
| | | Ch. Type | SE/ DIFF | SE/ DIFF | DIFF | DIFF | DIFF |
| | AC | SNR: 68dB | | | | | |
| | | ENOB: 10.5 bits | | | | | |
| **External TTL Trigger Input** | Low | 0.8 V max. | | | | | |
| | High | 2.4 V min. | | | | | |
| | Min. pulse width: 50ns | | | | | | |

## A.2 Analog Output

| | | |
|---|---|---|
| **Channels** | 2 | |
| **Resolution** | 12-bit | |
| **FIFO Size** | 4k samples | |
| **Output Rate** | 250 kS/s | |
| **Output Range** | Using Internal Reference | 0~5, 0~10, ±5, ±10 V |
| | Using External Reference | 0 ~ +x V @ +x V (-10 ≤x ≤10)<br>-x ~ +x V @ +x V (-10 ≤x ≤10) |
| **Slew Rate** | 20 V/μs | |
| **Accuracy** | Relative | ±1 LSB |
| | Differential Non-linearity | ±1 LSB (monotonic) |
| **Gain Error** | Adjustable to zero | |
| **Drift** | 10 ppm / °C | |
| **Driving Capability** | 10 mA | |
| **Update Rate** | Static update, waveform | |
| **Output Impedance** | 0.1 ohm max. | |

## A.3 Digital Input/Output

| | | |
|---|---|---|
| **Channels** | 16 (shared), TTL compatible | |
| **Input Voltage** | Low | 0.8V max. |
| | High | 2.4 V min. |
| **Output Voltage** | Low | 0.8 V max.@ +8.0mA (sink) |
| | High | 2.4 V min.@ -0.4mA(source) |

## A.4 Counter/Timer

| | | |
|---|---|---|
| **Channels** | 3 (independent) | |
| **Resolution** | 24-bit | |
| **Compatibility** | TTL level | |
| **Base Clock** | Internal 20 MHz or external clock(10 MHz max.), selected by software | |
| **Max. Input Frequency** | 10 MHz | |
| **Clock Input** | Low | 0.8 V max. |
| | High | 2.4 V min. |
| **Clock Input** | Low | 0.8 V max. |
| | High | 2.4 V min. |
| **Counter Output** | Low | 0.8 V max.@+24 mA |
| | High | 2.4 V min.@-15 mA |
| **Error in Advanced Functions*** | Freq. Measurement | ±10 ppm when input signal frequency > 500KHz |
| | Pulse Width Measurement | up to 50% when input signal frequency > 1MHz |
| | Pulse Output | within 2% when output frequency > 1MHz |
| | PWM Output | within 2% when output frequency > 1MHz |

**Note: When performing advanced functions, like frequency measurement and pulse output, there will be errors. And the error will vary depending on the parameter selections and the OS performance.*

## A.5 General

| | | |
|---|---|---|
| **I/O Connector Type** | 50-pin and 26-pin box header | |
| **Dimensions** | 96 x 90 mm (3.8" x 3.5") | |
| **Power Consumption** | **Typical** | +5 V @ 850 mA |
| | **Max.** | +5 V @ 1 A |
| **Temperature** | **Operating** | 0~60° C (32~140° F)<br>(refer to *IEC 68-2-1,2)* |
| | **Storage** | -20~ 70° C (-4~158° F) |
| **Relative Humidity** | **Operating** | 5~85%RH non-condensing<br>(refer to *IEC 68-1,-2,-3*) |
| | **Storage** | 5~95%RH non-condensing<br>(refer to *IEC 68-1,-2,-3*) |
| **Certifications** | CE/FCC certified | |

APPENDIX B

# Operation Theory

# Appendix B Operation Theory

## B.1 Analog Input Operation

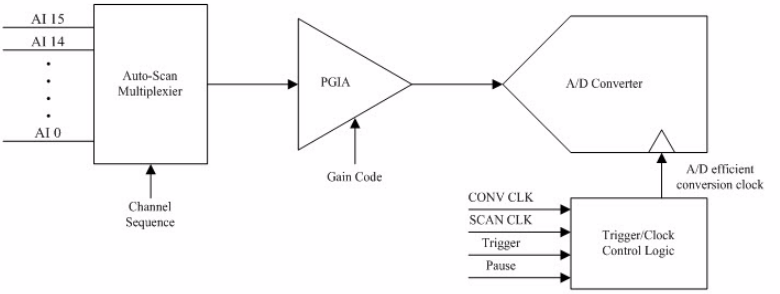
This section describes the following features of analog input operation theory that can help you realize how to configure the functions and parameters to match various applications.

- A/D Hardware Structure
- Analog input ranges and gains
- Analog data acquisition mechanism
- Analog input acquisition modes
- A/D SCAN/CONV clock source
- A/D trigger sources
- Analog input data format

### B.1.1 A/D Hardware Structure

The A/D conversion hardware structure includes four major parts:

- **Auto-scan multiplexer** routes the analog input signals into A/D converter channel by channel in a software-defined sequence.
- **PGIA** (Programmable Gain Instrument Amplifier) rectifies the input range and amplify/alleviate input signal to match the input range of A/D converter.
- **A/D converter** conceives the rectified voltage from **PGIA** and transfers it into the corresponding digital data format.
- **Trigger/Clock control logic** enables/disables the whole process and determines acquisition timing interval.




A/D Conversion Hardware Structure

## B.1.2 Analog Input Ranges and Gains

The PCM-3810I can measure both unipolar and bipolar analog input signals. A unipolar signal can range from 0 to 10 V FSR (Full Scale Range), while a bipolar signal extends within ±10 V FSR. The PCM-3810I provides various programmable gain levels and each channel is allowed to set its own input range individually. Table B.1 lists the effective ranges supported by the PCI-3810I with gains.

***Table B.1: Gains and Analog Input Range***

| Gain | Unipolar Analog Input Range | Bipolar Analog Input Range |
|---|---|---|
| 0.5 | N/A | ± 10 V |
| 1 | 0 ~ 10 V | ± 5 V |
| 2 | 0 ~ 5 V | ± 2.5 V |
| 4 | 0 ~ 2.5 V | ± 1.25 V |
| 8 | 0 ~ 1.25 V | ± 0.625 V |

For each channel, choose the gain level providing the most optimal range that can accommodate the signal range you want to measure.

## B.1.3 Analog Input Acquisition Mode

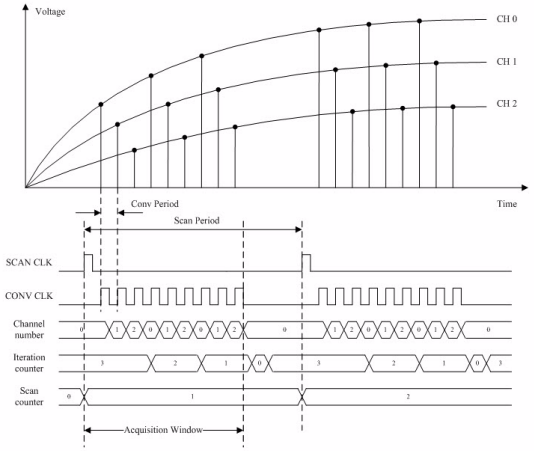
The PCM-3810I can acquire data in either single value or pacer mode.

- **Single Value Acquisition (Polling) Mode**
  The single value acquisition mode is the simplest way to acquire data. User can simply poll the data register of the desired channel to get the latest acquired value. Each analog input channel has its own dedicated data register (buffer) and in this mode the PCM-3810I updates each channel cyclically. The update rate is *sampling rate/num. of active channels.*

- **Pacer Acquisition Mode**
  Adopt pacer acquisition mode to acquire data if you wanna accurately control the time interval between conversions. A/D conversion clocks come from internal clock sources or external signals on connector. A/D conversion starts when the clocks signal come in, and will not stop if the clocks are continuously sent. Conversion data is accumulated into the on-board A/D buffer and waiting the transfer to PC memory. Further, you can specify Trigger and Pause gate to acquire the desired periods. We will discuss the detail in the next sections.

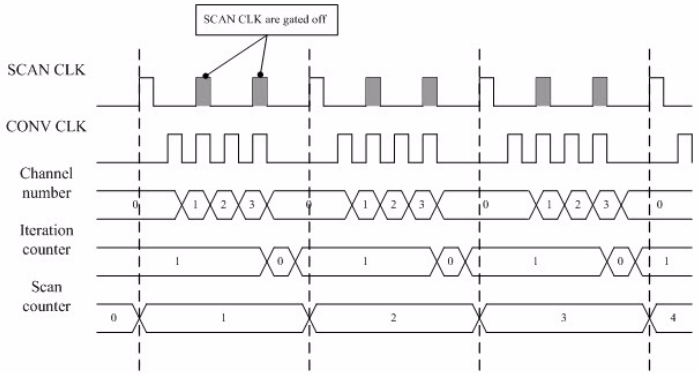
- **A/D Data Acquisition Clock Timing**
  The PCM-3810I introduces a double-clock system, with SCAN clock and CONV clock, to generate efficient A/D conversion clocks at dedicated timing. You can control acquisition timing interval precisely and just acquire the desired period. It can save the waste of PCI bandwidth with continuing acquisition and post data processing by filtering-out the redundant data beforehand. In this section, we will describe how it works and its timing reference in detail.

- **Double-Clock Procedure**
  Double clock procedure is the fundamental A/D conversion mechanism of the PCM-3810I, regardless of which mode selected. The incoming SCAN CLK launches an acquisition period called **Acquisition Window**. The arriving CONV CLKs within the **Acquisition Window** will become an efficient A/D conversion clock to trigger A/D converter. The number of efficient CONV CLK depends on the number of active scanning (multiplex) channels and software-programed iteration counters. One scanning iteration is defined as the time auto-scan multiplexer routes input channels from Start channel to Stop channel once. On the other words, all the active channels are sampled once in a single iteration. After the iteration counter counts down to zero, the Acquisition Window will be disable automatically and wait for the next incoming SCAN CLK. The end of Acquisition Window resets the iteration counter to its user-specified value. Users can specify the iteration counter by software and read back the number of incoming SCAN CLKs from SCAN CLK counter.

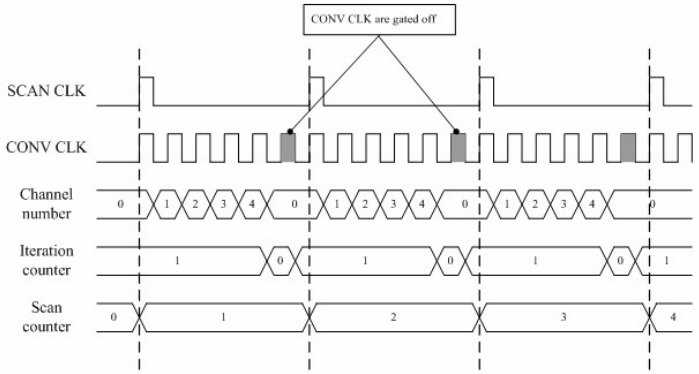



Double Clock timing Diagram

Once the acquisition procedure inside Acquisition Windows is set, the incoming CLKs must fit in the user-specified acquisition sequence, or the CLKs may be gated off. Refer to the following figures for more details.

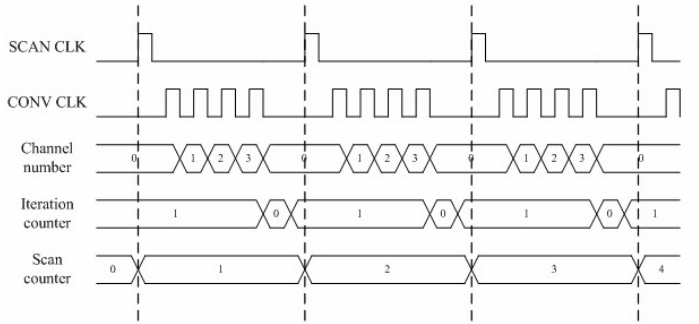



SCAN CLK is too fast

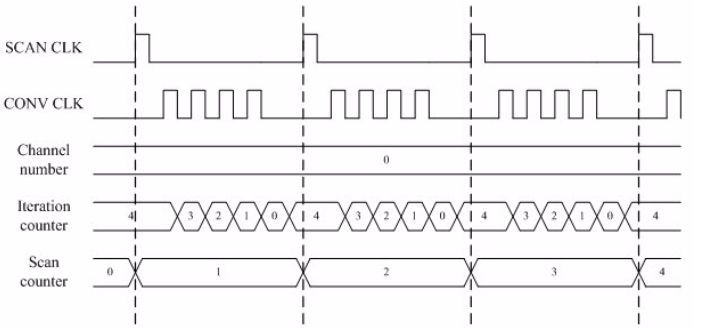



CONV CLK is too fast

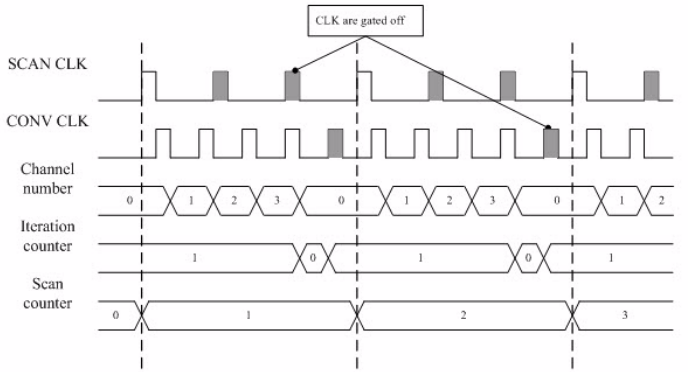
Other scanning procedure applications timing diagram.




Single Iteration

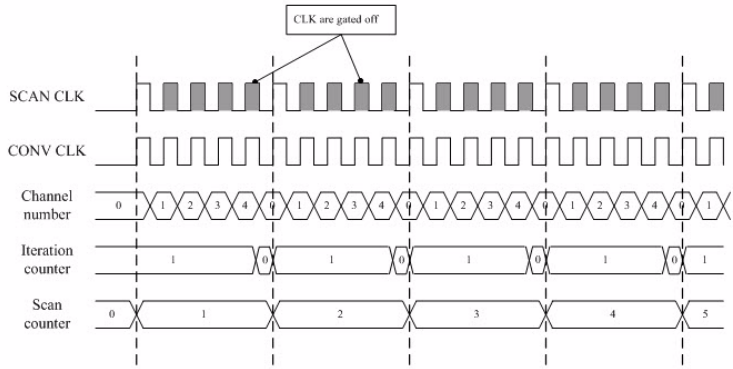



Multiple Iteration timing with fixed channel




Improperly matched SCAN CLK and CONV CLK

- **Single Clock Source Driving**
  Single clock source driving is a specific function well-suited for consecutive data acquisition while there is only one clock signal available. CONV CLKs will be internally routed as SCAN CLKs. And the external SCAN CLKs input will not be accepted. Figure describes how it works.

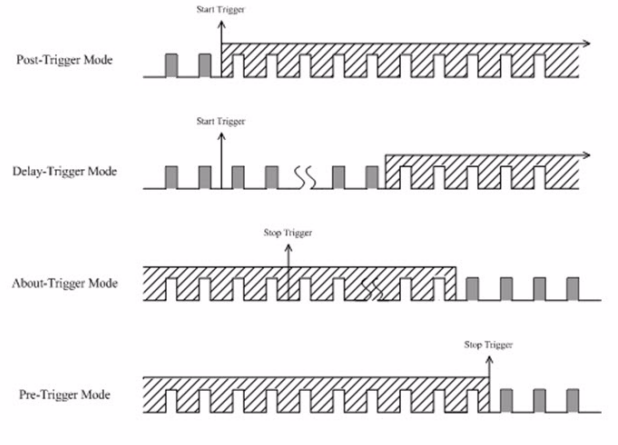



Single clock source driving both CLKs

## B.1.4 A/D Trigger Modes and Pause Gate

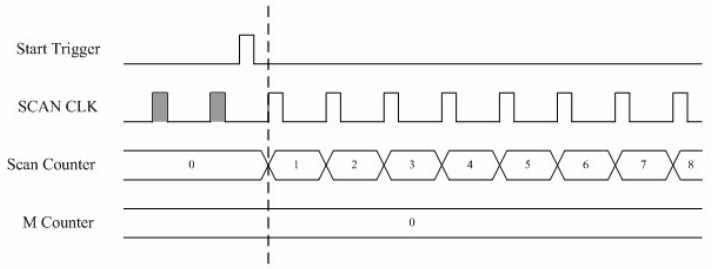
The PCM-3810I supports four trigger modes and pause function. User can start or stop the operation by trigger mode selection. An extra 32-bit counter is dedicated to delay-trigger mode and about-trigger mode, and user can set it as the number of delay SCAN CLKs before trigger or the number of holding SCAN CLKs after trigger. Figure shows the four different trigger modes.

Pause gate function provides a way to control the acquisition period directly from external hard-wiring. Once pause gate is asserted, the incoming SCAN CLKs will be blocked. The trigger edge and pause priority can be set by software. In the following figures, we assume a positive-going active edge and high-level priority.



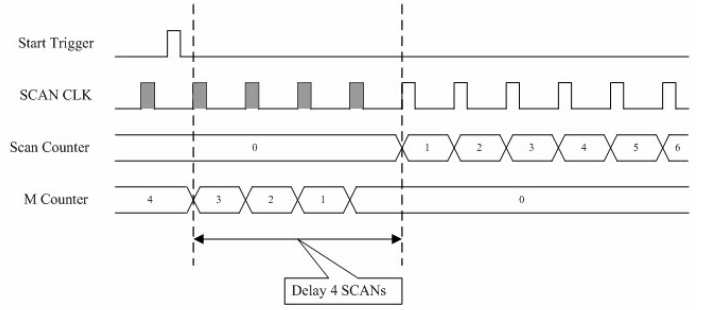

Trigger Modes

- **Post Trigger Acquisition Mode**
  Post-trigger acquisition starts when the PCM-3810I detects the trigger event and stops when you stop the operation. The SCAN CLKs before Trigger will be blocked out. You can set post-trigger acquisition mode by software.



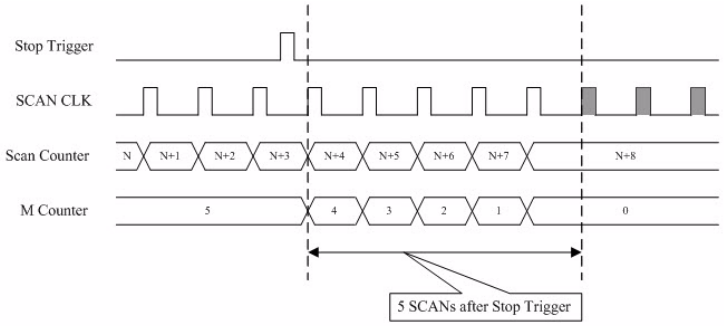

Post Trigger ( M = 0 )

- **Delay Trigger Acquisition Mode**
  In delay trigger mode, data acquisition will be activated after a preset delay number of SCAN CLKs has been taken after the trigger event. User can set the delay number of SCAN CLKs by a 32-bit counter. Delay-trigger acquisition starts when the PCM-3810I detects the trigger event and stops when you stop the operation.



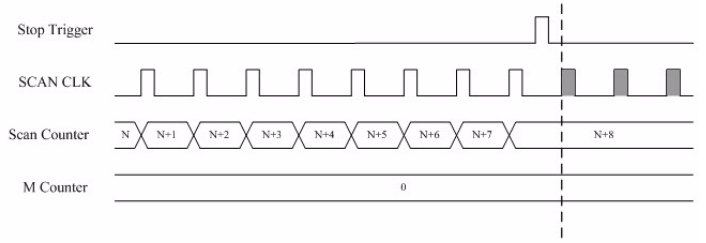

Delay Trigger ( M = 4 )

- **About Trigger Acquisition Mode**
  When you want to acquire data both before and after a specific trigger event occurs, users should take advantage of the about-trigger mode. First designate the size of the allocated memory and the amount of samples to be snatched after the trigger event happens. The about-trigger acquisition starts when the first SCAN CLK signal comes in. Once a trigger event happens, the on-going data acquisition will continue until the designated amount of SCAN CLKs have been reached. When the PCM-3810I detects the selected about-trigger event, the card keeps acquiring the preset number of samples, and kept them on the buffer.



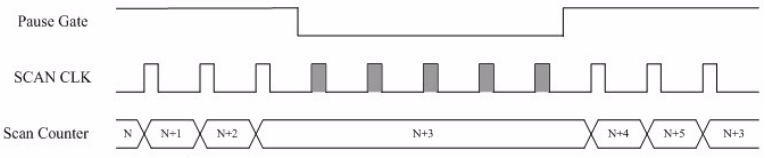

About-Trigger ( M = 5 )

- **Pre Trigger Acquisition Mode**
  Pre-Trigger mode is a particular application of about-trigger mode. Use pre-trigger acquisition mode when you want to acquire data before a specific trigger event occurs. Pre-trigger acquisition starts when you start the operation and stops when the trigger event happens.




Pre-Trigger ( M = 0 )

- **Pause Gate Intervene**
  The pause gate can be applied to block the incoming SCAN CLKs temporarily. You can set high-level pass or low-level pass to gate out the incoming SCAN CLKs. You can enable pause gate by software.




Pause Gate

## B.1.5 A/D SCAN/CONV Clock Source

The PCM-3810I can adopt both internal and external clock sources to accomplish pacer acquisition. You can set the clock and trigger sources conveniently by software. The figure can help you understand the routing route of clock and trigger generation.

**SCAN Clock**

- Internal A/D SCAN clock derived from 32-bit divider
- External A/D SCAN clock from terminal board
- External A/D CONV clock from terminal board

- **Internal A/D SCAN Clock**
  The internal A/D SCAN clock uses a 20 MHz time base divided by a 32-bit divider programmable by software. You can program SCAN clock source to internal and its frequency the clock source as internal and the frequency, 250 KS/s maximum, to activate A/D conversions.. To ensure system stability, SCAN clock frequency should be less or equal to CONV clock.

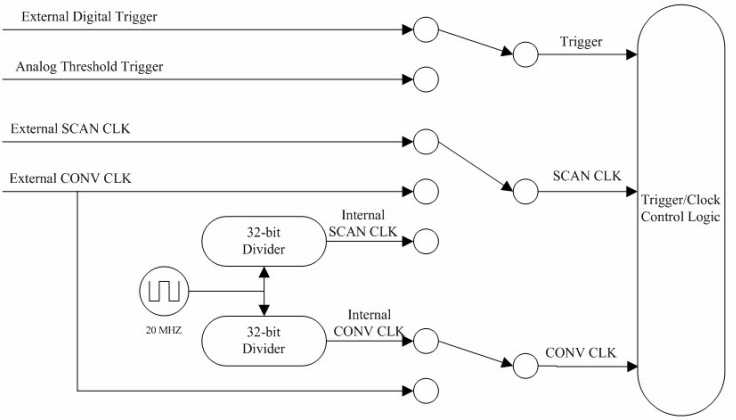
- **External A/D SCAN Clock**
  The external A/D SCAN clock is useful when you want to execute acquisitions at rates not available from the internal A/D SCAN clock, or when you want to pace at uneven intervals. Acquisitions will start the rising edge of the external A/D SCAN clock input. And the frequency should be always limited under 250 KHz. The exceeding frequency may result in data loss or unexpected data acquisition.

- **External A/D CONV clock**
  This setting is useful when single external clock source is available. Instead of hard-wire, the internal routing can protect signals from different line transmission delay.

  **CONV Clock**
  - Internal A/D CONV clock derived from 32-bit divider
  - External A/D CONV clock from terminal board

- **Internal A/D CONV Clock**
  The same as internal SCAN clock, the internal A/D CONV clock applies 20 MHz time base accompanied with 32-bit divider. The maximum frequency is 250 KS/s. According to the sampling theory (Nyquist Theorem), you must specify a frequency that is at least twice as fast as the input's highest frequency component to achieve a valid sampling. For example, to accurately sample a 20 kHz signal, you have to specify a sampling frequency of at least 40 kHz. This consideration can avoid an error condition often know as aliasing, in which high frequency input components appear erroneously as lower frequencies when sampling.

- **External A/D CONV Clock**
  The external A/D CONV Clock is convenient in uneven sampling internal. A/D conversion will start by each arriving rising edge. The sampling frequency is always limited to a maximum of 250 KHz.




Trigger/Clock Routing Diagram

## B.1.6 A/D Trigger Source

The PCM-3810I supports the following trigger sources for post-, delay-, about- and pre-trigger acquisition modes:

- External digital (TTL) trigger
- Analog threshold trigger

With PCM-3810I, user can also define the type of trigger source as rising-edge or falling-edge. These following sections describe these trigger sources in more detail.

- **External Digital (TTL) Trigger**
  For analog input operations, an external digital trigger event occurs when the PCM-3810I detects either a rising or falling edge on the External A/D TTL trigger input. The trigger signal is TTL compatible.

- **Analog Threshold Trigger**
  For analog input operations, an analog trigger event occurs when the PCM-3810I detects a transition from above a threshold level to below a threshold level (falling edge), or a transition from below a threshold level to above a threshold level (rising edge). User should connect analog signals from external device or analog output channel on board to external input signal ANA_TRG. On the PCM-3810I, the threshold level is set using a dedicated 8-bit DAC. By software, you can program the threshold level by writing a voltage value to this DAC; this value can range from -10 V to +10 V.

***Table B.2: Analog Input Data Format***

| A/D Code | | Mapping Voltage | |
|---|---|---|---|
| Hex. | Dec. | Unipolar | Bipolar |
| 000 h | 0 d | 0 | -FS/2 |
| 7FFF h | 2047 d | FS/2 - 1 LSB | - 1LSB |
| 800 h | 2048 d | FS/2 | 0 |
| FFF h | 4095 d | FS - 1 LSB | FS/2 - 1 LSB |
| 1 LSB | | FS/4096 | FS/4096 |

***Table B.3: Full Scale Values for Input Voltage Ranges***

| Gain | Unipolar | | Bipolar | |
|---|---|---|---|---|
| | Range | FS | Range | FS |
| 0.5 | N/A | N/A | ± 10 V | 20 |
| 1 | 0 ~ 10 V | 10 | ± 5 V | 10 |
| 2 | 0 ~ 5 V | 5 | ± 2.5 V | 5 |
| 4 | 0 ~ 2.5 V | 2.5 | ± 1.25 V | 2.5 |
| 8 | 0 ~ 1.25 V | 1.25 | ± 0.625 V | 1.25 |

## B.2 PCM-3810I Analog Output Operation

The PCM-3810I card provides two 12-bit multi-range analog output (D/A) channels. This section describes the following features:

- Analog output ranges
- Analog output operation modes
- Synchronous Analog output waveform
- D/A clock sources
- D/A Trigger sources
- Analog Output Data Format

### B.2.1 Analog Output Ranges

The PCM-3810I provides two 12-bit analog output channels, both of which can be configured internally to be applicable within 0 ~ 5 V, 0 ~ 10 V, ± 5 V, ± 10 V output voltage range. Otherwise, users can use external reference voltage to apply 0 ~ x V or ± x V output range, where the value x is from -10 to +10. Users can configure the output range during driver installation or in software programming.

### B.2.2 Analog Output Operation Modes

- **Single Value Operation Mode**

The single value conversion mode is the simplest way for analog output operation. Users can set the mode of each channel individually. Then users just need to use software to write output data to specific register. The analog output channels will output the corresponding voltage immediately. In the single value operation mode, users need not set any clock source and trigger source, but only output voltage range.

- **Continuous Output Operation Mode**
  In continuous output operation mode, users can accurately control the update rate (up to 250 kS/s) between conversions of individual analog output channels, and takes full advantage of the PCM-3810I. In this mode you can specify a clock and trigger source and either of the two analog output channels to work in this mode. But when both of them operate in this mode, the maximum update rate will be 125 kS/s for each.

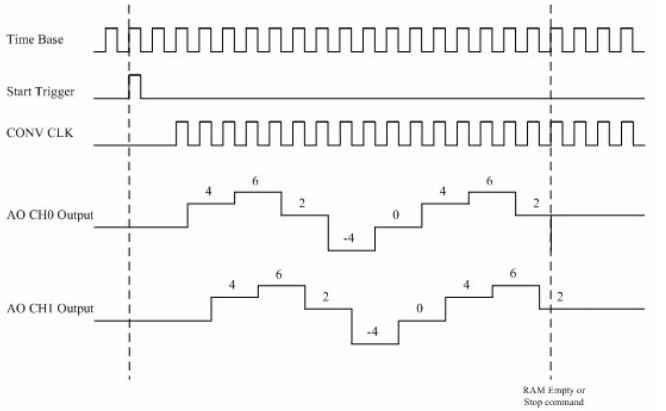
Before operating in this mode, users need to set the clock and trigger source first, and then generate the output data stored in the memory buffers of host PC. The host computer then transfers those data to the DACs' buffers on PCM-3810I. When PCM-3810I detects a trigger, it outputs the values stored in its buffer. When the buffer's storage decreases, the card sends an interrupt request to the host PC which in turn sends samples to the buffer. This output operation will repeat until either all the data is sent from the buffers or until you stop the operation. If the two D/A channels are both operating in continuous output mode, the data in buffer will be sent in an interlaced manner, i.e. the "Even-Address" samples in the buffer are sent to D/A channel 0, while the "Odd-Address" samples to D/A channel 1.

- **Waveform Output Operation Mode**

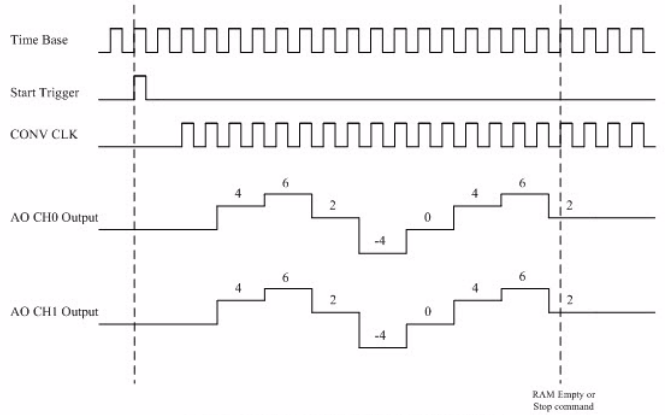
  Waveform output operation mode is a particular and useful application of continuous output operation mode. In this mode, users can output the user-defined waveform pattern repetitively and continuously. Before this operation begins, users have to use software to allocate the buffer memory and define the waveform pattern first. Then the host computer will transfer the waveform pattern from its buffer allocated in computer memory into the Output buffer on the board, which in turn will transfer the waveform pattern to the DACs. When the trigger event occurs, each D/A channel running continuous output operation mode will output waveform pattern from buffer in specific clock rate.

- **Synchronous Analog Output Waveform**

  All D/A channels can change output voltage at the same time, while the synchronous waveform output feature is armed. Once this feature enabled, each DAC will hold on its value and wait until the last DAC receives data from buffer. Then all channels will deliver their own output voltage simultaneously. The update rate will be divided by the number of active AO channels at the same time. The following figures show the waveform and timing difference between synchronous and asynchronous output.




Asynchronous Analog Waveform output




Synchronous Analog Waveform output

### B.2.3 D/A Clock Sources

The PCM-3810I can adopt both internal and external clock sources for pacing the analog output of each channel:

- Internal D/A output clock with 32-bit Divider
- External D/A output clock from connector

The internal and external D/A output clocks are described in more detail as follows:

- **Internal D/A Output Clock**
  The internal D/A output clock applies a 20 MHz time base divided by a 32-bit counter. Conversions start on the rising edges of counter output. Through software, user can specify the clock source and clock frequency to pace the analog output operation. The maximum frequency is 250 kS/s.

- **External D/A Output Clock**
  The external D/A output clock is useful when you want to pace analog output operations at rates not available with the internal D/A output clock, or when you want to pace at uneven intervals. Connect an external D/A output clock to the pin and then the conversions will start on input signal's rising edge. You can use software to specify the clock source as external. The maximum input clock frequency is 250 kS/s.

### B.2.4 D/A Trigger Sources

The PCM-3810I supports External digital (TTL) trigger to activate D/A conversions for continuous output mode. An external digital trigger event occurs when the PCM-3810I detects either a rising or falling edge on the External D/A TTL trigger input signal from the pin of connector. User can define the type of trigger source as rising-edge or falling-edge by software. The trigger signal is TTL-compatible.

***Table B.4: Analog Output Data Format***

| D/A code | | Mapping Voltage | |
|---|---|---|---|
| Hex. | Dec. | Unipolar | Bipolar |
| 000 h | 0 d | 0 | -FS/2 |
| 7FF h | 2047 d | FS/2 - 1 LSB | -1 LSB |
| 800 h | 2048 d | FS/2 | 0 |
| FFF h | 4095 d | FS - 1 LSB | FS/2 - 1 LSB |
| 1 LSB | | FS/4096 | FS/4096 |

***Table B.5: Full Scale Values for Output Voltage Ranges***

| Reference Source | Unipolar | | Bipolar | |
|---|---|---|---|---|
| | Range | FS | Range | FS |
| Internal | 0~ 5 V | 5 | ± 5 V | 10 |
| | 0~ 10 V | 10 | ± 10V | 20 |
| External | 0~ x V | x | ± x V | 2x |

## B.3 Digital Input/Output Operation

The PCM-3810I supports 16 digital I/O channels. These I/O channels are divided into two bytes: specifically a low byte, DIO0 to DIO7; and a high byte, DIO8 to DIO15. You can use each byte as either an input port or an output port by configuring the corresponding parameter; and all eight channels of the byte have the same configuration.

You do not need to specify the clock source or trigger source. To output the data, you just need to write it to the digital output channel directly. In the same way, you can directly read back data from digital input channel. The default configuration after reset sets all the digital I/O channels to logic-low so users don't need to worry about damaging external devices during system start up or reset.

## B.4 Counter Function

The PCM-3810I provides three 24-bit powerful counters fulfilling variant requirements. Each counter has clock input, gate input and pulse output. They can operate independently or cascade with one another. Each of them can be programmed to count up to 16,777,215.

**Features**

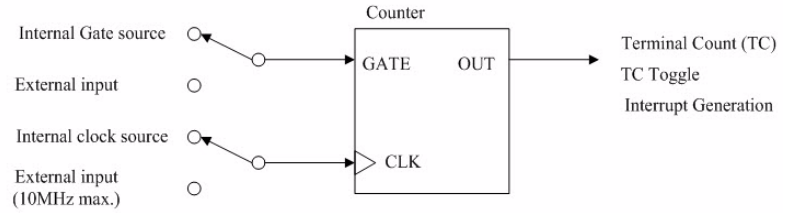
- 3 independent 24-bit counters
- Maximum internal 20MHz or external 10Mhz input frequency
- Multiple counter clock source selectable
- Counter output programmable
- Counter gate function

**Applications**

- Event counting
- One shot output
- Pulse out
- PWM output
- PWM input/Pulse width measurement
- Frequency measurement
- Timer interrupt

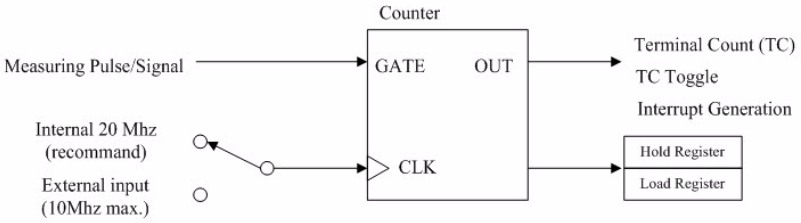
## B.4.1 Signal Connections

- **Basic Operation Connection**




Here the general counter applications are implemented including event counting, one shoot, pulse out, one shot output, PWM output, and timer interrupt generation. Input clock\gate signals into the corresponding ports CLK\GATE to get the desired results from the output port, OUT, directly. Various clock and gate sources are supplied internally to fulfill different timing length and accuracy requirements. And output is also programmable to practice different purposes.

- **Pulse Width/Frequency Measurement**




This connection is suitable for the measurement of pulse width and frequency. Connect the pulse-width-unknown signal to counter's GATE input, and then counter itself will automatically save the pulse width information into its internal registers. Up cycle period is stored in Hold register and down cycle period is in Load register. The duty cycle can also be calculated easily by dividing the up period by the total period (up period + down period). Internal 20 MHz clock is highly recommended for the precise measurement.

## B.4.2 Clock Sources

The following clock sources are available for the user counters, and they are available to set its active edge as rising edge or falling edge:

- **Internal Clock**
  Users can specify the internal clock ranging from 2Hz to 20MHz as the clock source through programming.

- **External Clock**
  The external clock is useful when you want to pace counter/timer operations at rates not available with the internal clock or if you want to pace at uneven internals. The maximum frequency of the external clock is limited to 10Mhz. The over-frequency clock will cause unpredictable result or error.

- **Internally Cascaded Clock**
  You can also route the clock output from the counter to the next counter's clock input to internally cascade the counters. In this way, you can create a 48-bit or even a 72-bit counter without externally cascading multiple counters.

## B.4.3 Gate Types and Sources

The gate type and source you select determine the functionality and the behavior of your counter/timer. There are four different gate types on the list including No Gating, Level Gate, Edge Gate, and Pulse Mode. Each of them manipulates the counter\timer in different operations and procedures. You can refer to Counter Mode Table and the timing diagram to help you find the suitable choice.

- **No Gating**
  After being issued, the counter/timer will count every clock(CLK) edges regardless of the Gate input. Once counting down/up to zero, the counter/timer will reload from Load or Hold register at the next coming clock edge automatically.

- **Level Gate**
  The operation is similar to No Gating type under the Gate's escort. The active level presenting on the Gate will succeed the desired incoming source edges and the opposite level blocks the unwanted clock. Active Gate level could be high-logic or low-logic defined by software-setting Gate priority register.

- **Edge Gate**
  Once issued *Edge Gate*, the counter/timer waits the arriving active edge to activate the counting. Without it, the counter/timer will just be suspended. This is quite useful when you want to trigger the timer multiple times between variant intervals. Active Gate edge could also be positive-going or negative-going.

- **Pulse Mode**
  Different from other types, *Pulse Mode* dedicates a specific counting process for frequency/pulse width measurement. While connecting the waveform you want to know into Gate, the counter will record the waveform's length and inform each update (transition) to the output. You can read back the up cycle period from the **Hold** register and the down cycle period from the **Load** register. Proper clock source selection determines the measuring timing resolution. Internal 20 MHz clock source is recommended in this mode.

The gate sources are described as follows.

- **External Gate Source**
  User can connect an external gate signal to its counter Gate pin or previous counter Gate pin. The previous counter of counter 0 is counter 2, of counter 1 is counter 0 and of counter 2 is counter 1. You can select the Gate source by software programming.
- **Previous Counter Output**
  User can use previous counter's output as your gate source to cascade multiple counters.

### B.4.4 Counter Output

While counting down/up to zero in *No Gating, Level Gate*, and *Edge Gate* or encountering a Gate logic transitions in P*ulse Mode*, the corresponding counter generates the output signal to inform user its current status. Two kinds of output signals, terminal count and terminal count toggle are described as follows.

- **Terminal Count (TC)**
  Counter yields a single pulse on Output when the counting-to-zero criteria are matched. User can set high-pulse or low-pulse terminal count output by software.

- **Terminal Count Toggle**
  While counting to zero, counter converts output logic level instead of a single pulse. The initial level can be defined by software.

- **Interrupt Generation**
  The positive-going edge of the output signal can trigger interrupt if the counter enables interrupt beforehand. Each counter has its own interrupt enable and interrupt flag.

### B.4.5 Counter/Timer Operation Applications

Through the multiple gate functions, it's easier to achieve various applications.Here we take some primary applications for your reference, including, event counting, one shoot, Pulse output, PWM output, Timer interrupt generation, and frequency/pulse width measurement. The detail control flow and corresponding waveform can be found in the software manual and next section. The following paragraphs briefly describe these applications.

- **Event Counting**
  The event counting application helps user count events from the counter's clock input. Each counter features 24-bit, and therefore you can count a maximum of 16,777,215 events before the counter overflows and returns to 0. If you need wider range for event counting, you can cascade multiple counters.

- **One Shoot**
  Counter generates a single pulse signal after counting for a while. You can use this pulse output signal as an external digital (TTL) trigger source to start other operations, such as analog input or analog output operations. Refer to Mode A and Mode G in next sections for detail information.

- **Pulse Output**
  Pulse output is similar to One Shoot except non-stop counting and iterative pulse output. User can refer it from Mode D.

- **Timer Interrupt Generation**
  Timer interrupt generation is the same as pulse output, except interrupt is enabled. Note that interrupt is only generated on output positive-going edge.

- **PWM Output**
  PWM (Pulse-width modulation) of a signal or power source involves the modulation of its duty cycle to either convey information over a communications channel or control the amount of power sent to a load. The term duty cycle describes the proportion of up cycle period to the whole period. User can set up cycle period and down cycle period respectively from **Hold** and **Load** registers.

- **Frequency/Pulse Width Measurement (PWM in)**
  The frequency/pulse width measurement function helps user to measure incoming signal to decode or acquire information.. Set as Pulse Mode, counter records up cycle period and low cycle period in internal Hold and Load Registers. User can derive signal frequency, pulse width, and duty cycle from these data. Refer to Mode X2, Mode X3, and software manual for detail information.

### B.4.6 Counter Mode Table

Here lists various counter modes corresponding to different applied situations. We will show their waveforms, parameters setting, and applications lately to help you clarify your requirement and set it up effectively.

(**N**: No gate control, **L**: Level gate control, **E**: Edge gate control, **P**: Pulse Width Measurement)

| Counter Mode | A | B | C | D | E | F | G | H | I | J | K | L |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Repetition (CM2) | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 |
| Reload Source (CM3) | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| Gate Mode (GM1~GM0) | N | L | E | N | L | E | N | L | E | N | L | E |
| Count to TC once, then disarm | ✓ | ✓ | ✓ | | | | | | | | | |
| Count to TC twice, then disarm | | | | | | | ✓ | ✓ | ✓ | | | |
| Count to TC repeatedly without disarming | | | | ✓ | ✓ | ✓ | | | | ✓ | ✓ | ✓ |
| Gate input dose not gate counter input | ✓ | | | ✓ | | | ✓ | | | ✓ | | |
| Count only during active gate level | | ✓ | | | ✓ | | | ✓ | | | ✓ | |
| Start count on active gate edge and stop count on next TC | | | ✓ | | | ✓ | | | | | | |
| Start count on active gate edge and stop count on second TC | | | | | | | | | ✓ | | | ✓ |
| Save counter value to Hold register on TC | | | | | | | | | | | | |
| Save counter value on TC, alternating save it to Hold and Load Registers. | | | | | | | | | | | | |
| Generate terminal count pulse while count to zero. | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | |
| Generate terminal count pulse while counter is actived and gate edge change | | | | | | | | | | | | |
| Reset counter value 0 on active gate edge and TC | | | | | | | | | | | | |
| Reload counter from Load Register on TC | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | | | | |
| Reload counter on each TC, alternating reload source between Load and Hold Registers | | | | | | | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |

| Counter Mode | X0 | X1 | X2 | X3 |
|---|---|---|---|---|
| Repetition (CM2) | 0 | 1 | 0 | 1 |
| Reload Source (CM3) | X | X | X | X |
| Gate Mode (GM1~GM0) | P | P | P | P |
| Count to TC once, then disarm | ✓ | | | |
| Count to TC twice, then disarm | | | ✓ | |
| Count to TC repeatedly without disarming | | ✓ | | ✓ |
| Gate input dose not gate counter input | | | | |
| Count only during active gate level | | | | |
| Start count on active gate edge and stop count on next TC | ✓ | ✓ | | |
| Start count on active gate edge and stop count on second TC | | | ✓ | ✓ |
| Save counter value to Hold register on TC | ✓ | ✓ | | |
| Save counter value on TC, alternating save it to Hold and Load Registers. | | | ✓ | ✓ |
| Generate terminal count pulse while count to zero. | | | | |
| Generate terminal count pulse while counter is actived and gate edge change | ✓ | ✓ | ✓ | ✓ |
| Reset counter value 0 on active gate edge and TC | ✓ | ✓ | ✓ | ✓ |
| Reload counter from Load Register on TC | | | | |
| Reload counter on each TC, alternating reload source between Load and Hold Registers | | | | |

### B.4.7 Waveform of Each Mode

PCM-3810I offers 16 powerful counter functions to fulfill your industrial or laboratory applications. This chapter will describe each mode in detail with the waveform diagram.

- **Counter Mode Descriptions**
  To simplify references to a particular mode, each mode is assigned a letter from A through L and X0 to X1. Representative waveforms for the counter modes are illustrated in Figure A through L and X0 to X1.

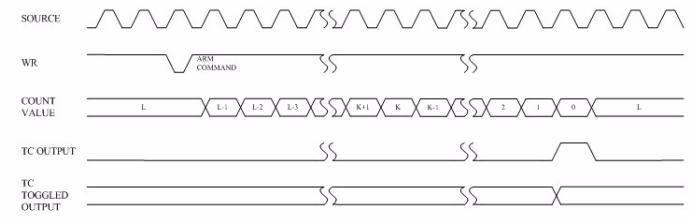
  The figures assume counting on rising source edges. Those modes, which automatically disarm the counter (Mode A, B, C, D, E, F, X0, X1) are shown with the WR pulse entering the required ARM command; for modes which count repetitively (Mode G, H, I, J, K, L, X2, X3) the ARM command is omitted. Both a TC output waveform and a TC Toggled output waveform are shown for each mode. Since PCM-3810I doesn't support hard-wired ARM input, driver will handle this command automatically. Please refer to software manual for the detail control flow.

  The symbols L and H are used to represent count values equal to the Load and Hold register contents, respectively. The symbols K, N, and R represent arbitrary count values. These figures are designed to clarify the mode descriptions.

  To keep the following mode descriptions concise and to the point, the phrase "source edges" is used to refer to active-going source edges only, not to inactive-going edges. Similarly, the phrase "gate edges" refers only to active-going gate edges. Also, again to avoid verbosity and euphuism, the descriptions of some modes state that a counter is stopped or disarmed "on a TC, inhibiting further counting."

  For these modes, the counter is actually stopped or disarmed following the active-going source edge which drives the counter out of TC. In other words, since a counter in the TC state always counts, irrespective of its gating of arming status, the stopping or disarming of the count sequence is delayed until TC is terminated.

- **Mode A Waveform**
  **Software-Triggered Strobe with No Hardware Gating**
  Mode A is one of the simplest operating modes. The counter will be available for countering source edges when it is issued and ARM command. On each TC the counter will reload from the **Load** register and automatically disarm itself, inhibiting further counting. Counting will resume when a new ARM command is issued.




Mode A Waveforms

**Repetition**: Disabled

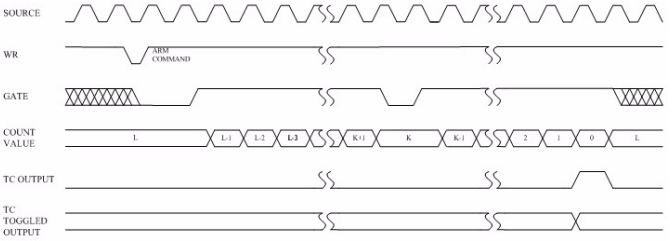
**Reload Source:** Load Register only

**Gate Mode:** No Gate control

- **Mode B Waveform**

  **Software-Triggered Strobe with Level Gating**

  Mode B is identical to Mode A except that source edges are counted only when the assigned Gate is active. The counter must be armed before counting can occur. Once armed, the counter will count all source edges that occur while the Gate is active and disregard those edges which occur while the Gate is inactive. This permits the Gate to turn the count process on and off. On each TC the counter will reload from the **Loa**d register and automatically disarm itself, inhibiting further counting until a new ARM command is issued.




Mode B Waveforms

**Repetition:** Disabled

**Reload Source:** Load Register only

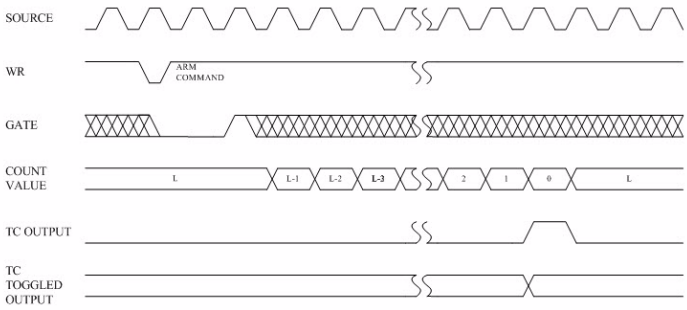
**Gate Mode:** Level Gate control

- **Mode C Waveform**
  **Hardware-Triggered Strobe**

  Mode C is identical to Mode A, except that counting will not begin until a Gate edge is applied to the armed counter, the counter must be armed before application of the triggering Gate edge; Gate edges applied to a disarmed counter are disregarded.

  The counter will start counting on the first source edge after the triggering Gate edge and will continue counting until TC. At TC, the counter will reload from the **Load** register and automatically disarm itself. Counting will then remain inhibited until a new ARM command and a new Gate edge are applied in that order.

  Note that after application of a triggering Gate edge, The Gate input will be disregarded for the remainder of the count cycle. This differs from Mode B, where the Gate can be modulated throughout the count cycle to stop and start the counter.




Mode C Waveforms

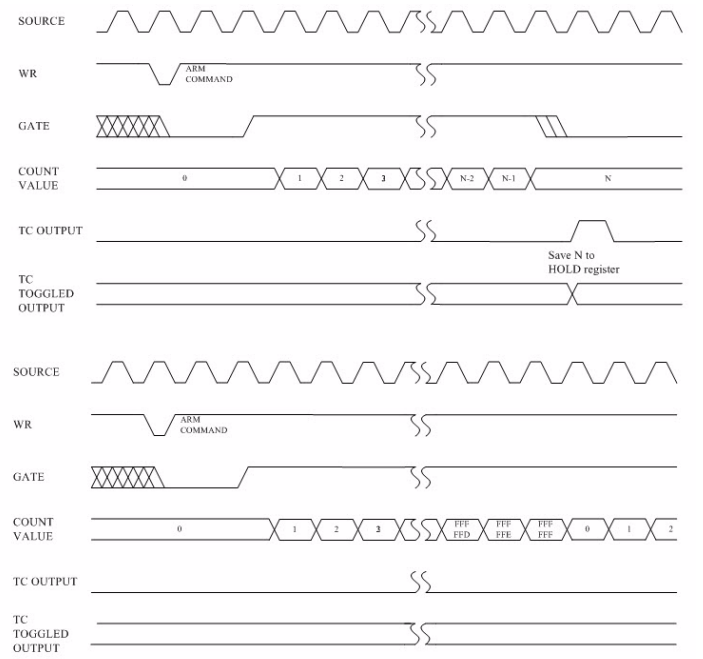
**Repetition:** Disable

**Reload Source:** Load Register only

**Gate Mode:** Edge Gate control

- **Mode X0 Waveform**
  **Pulse Width Measurement**

  Mode X0 provides single pulse length measurement function. The counter must be armed before the application of input pulse; the pulse applied to a disarmed counter is disregarded.
  The counter will start counting on the first source edge after the application of a Gate edge and will stop counting as the inactive Gate edge was applied. Then the counter will automatically store the finial value into Hold register, generate TC to inform the end of measurement, and finally disarm itself. Next measurement will then remain inhibited until a new ARM command and a new pulse is applied.
  Note that once the counting value is over the maximum capability (16,777,216), counter will ignore it and persist counting from 0. Slower clock frequency can be applied to avoid the overrun, but sacrifice the precision.




Mode D Waveforms

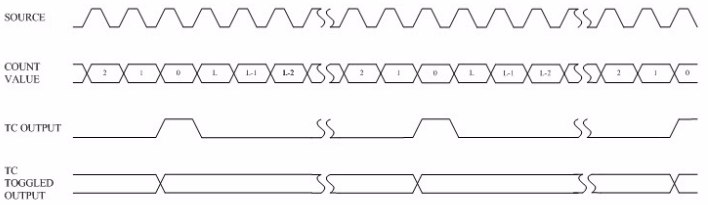
**Repetition:** Disable

**Reload Source:** Load Register only

**Gate Mode:** Pulse Width Measurement

- **Mode D Waveform**
  **Rate Generator with No Hardware Gating**

Mode D is typically used in frequency generation applications. In this mode, the Gate input does not affect counter operation. Once armed, the counter will count to TC repetitively. On each TC the counter will reload itself from the **Load** register; hence the **Loa**d register value determines the time between TCs. A square wave rate generator may be obtained by specifying the TC Toggled output.




Mode E Waveforms

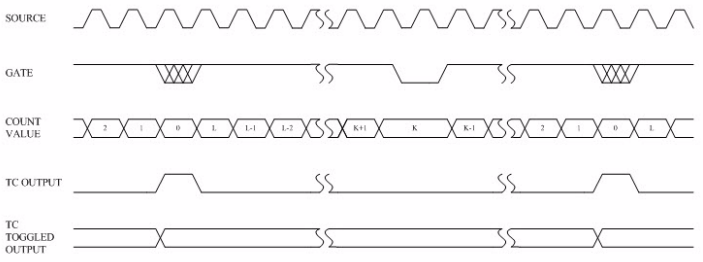
**Repetition:** Enable

**Reload Source:** Load Register only

**Gate Mode:** No Gate control

- **Mode E Waveform**
  **Rate Generator with Level Gating**

Mode E is identical to Mode D, except the counter will only count those source edges that occur while the Gate input is active. This feature allows the counting process to be enabled and disabled under hardware control. A square wave rate generator may be obtained by specifying the TC Toggled output mode.




Mode F Waveforms

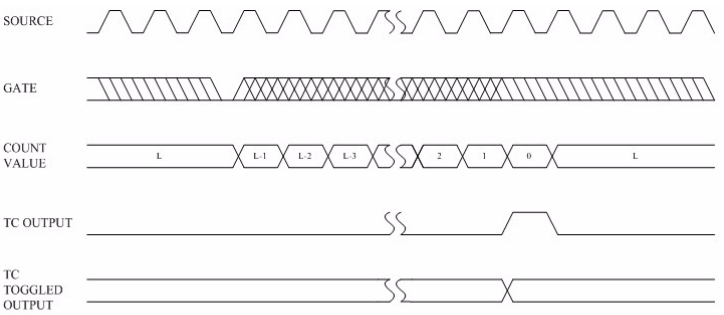
**Repetition:** Enable

**Reload Source:** Load Register only

**Gate Mode:** Level Gate control

- **Mode F Waveform**
  **Non-Retriggerable One-Shot**

  Mode F provides a non-retriggerable one-shot timing function. The counter must be armed before it will function. Application of a Gate edge to the armed counter will enable counting. When the counter reaches TC, it will reload itself from the **Load** register. Then the counter will stop counting, awaiting a new Gate edge. Note that unlike Mode C, a new ARM command is not needed after TC, only a new Gate edge. After application of a triggering Gate edge, the Gate input is disregard until TC.




Mode G Waveforms

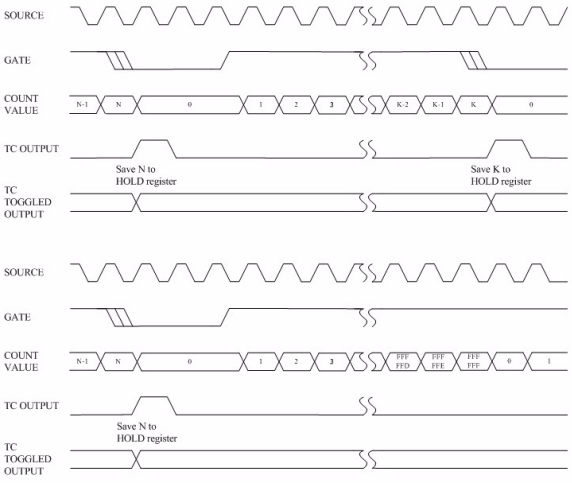
**Repetition:** Enable

**Reload Source:** Load Register only

**Gate Mode:** Edge Gate control

- **Mode X1 Waveform**
  **Continuous Pulse Width Measurement**

Mode X1 provides a consecutive mechanism to monitor the varied pulse width. The counter must be armed before it functions. Application of a Gate edge to the armed counter will enable the counting from zero. When the inactive Gate edge happens, the counter will automatically store the count value into **Hold** register and generate TC to inform the availability of the measurement result. Note that unlike Mode D, a new ARM command is not needed after TC, only a new arriving pulse.
Once the count value over the maximum capability (16,777,216), the counter will ignore the overrun and persist counting from 0. Slower clock frequency can be applied to avoid it, but sacrifice some precision.




Mode H Waveforms

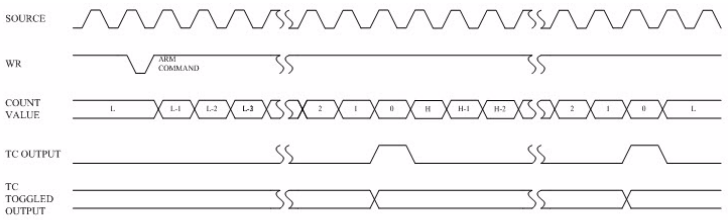
**Repetition:** Enable

**Reload Source:** Load Register only

**Gate Mode:** Pulse Width Measurement

- **Mode G Waveform**
  **Software-Triggered Delayed Pulse One-Shot**

  In Mode G, the Gate does not affect the counter's operation. Once armed, the counter will count to TC twice and then automatically disarm itself. For most applications, the counter will initially be loaded from the **Load** register either by a LOAD command or by the last TC of an earlier timing cycle.
  Upon counting to the first TC, the counter will reload itself from the **Hold** register. Counting will proceed until the second TC, and then the counter will reload itself from the **Load** register and automatically disarm itself, inhibiting further counting. Counting can be resumed by issuing a new ARM command.
  Specifying the TC Toggled output mode in the Counter Mode register may generate a software-triggered delayed pulse one-shot. The initial counter contends control of the delay from the ARM command until the output pulse starts. The **Hold** register contents control the pulse duration.




Mode I Waveforms

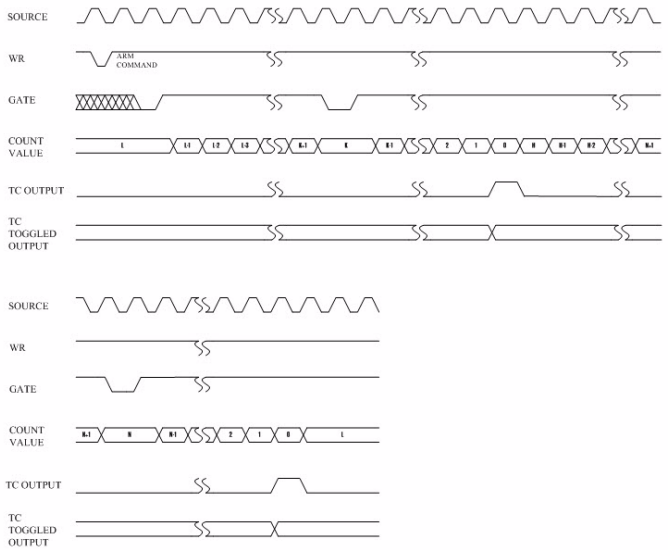
**Repetition:** Disable

**Reload Source:** Reload from LOAD or HOLD registers.

**Gate Mode:** No Gate control

- **Mode H Waveform**
  **Software-Triggered Delayed Pulse One-Shot w/ Hardware Gating**

  Mode H is identical to Mode G except that the Gate input is used to qualify which source edges are to be counted. The counter must be armed for counting initialization. Once armed, the counter will count all source edges that occur while the Gate is active and disregard those source edges that occur while the Gate is inactive. This permits the Gate to turn the count process on and off.
  As with Mode G, the counter will be reloaded from the **Hold** register on the first TC and reloaded from the **Load** register and disarmed on the second TC. This mode allows the Gate to control the extension of both the initial output delay time and the pulse width.




Mode J Waveforms

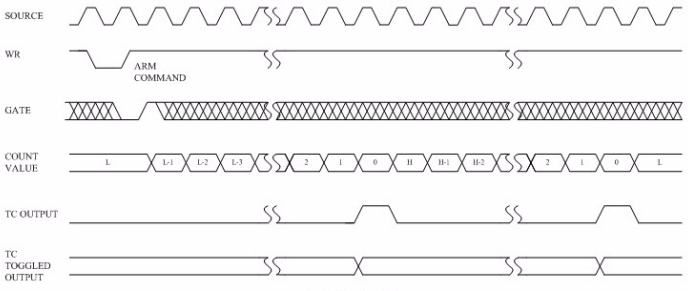
**Repetition:** Disable

**Reload Source:** Reload from LOAD or HOLD registers.

**Gate Mode:** Level Gate control

- **Mode I Waveform**
  **Hardware-Triggered Delayed Pulse Strobe**

  Mode I is identical to Mode G, except the counting will not begin until a Gate edge is applied to an armed counter. The counter must be armed before application of the triggering Gate edge; Gate edges applied to a disarmed counter are disregarded. An armed counter will start counting on the first source edge after the triggering Gate edge. Countering will then proceed in the same manner as in Mode G. After the second TC, the counter will disarm itself. An ARM command and Gate edge must be issued in this order to restart counting.
  Note that after application of a triggering Gate edge, the Gate input will be disregarded until the second TC. This differs from Mode L, where the Gate can be modulated throughout the count cycle to stop and start the counter.



Mode K Waveforms

**Repetition:** Disable

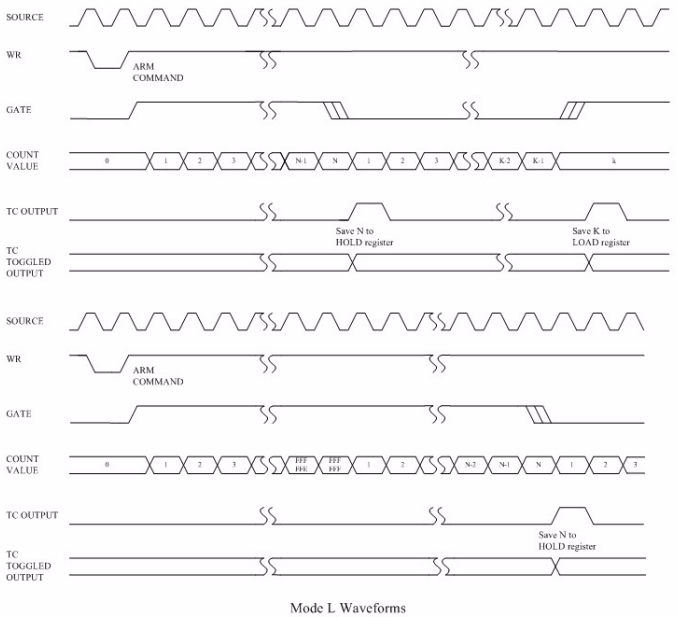
**Reload Source:** Reload from LOAD or HOLD registers.

**Gate Mode:** Edge Gate control

- **Mode X2 Waveform**
  **Signal Duty Cycle/Frequency Measurement (PWM in)**

  Mode X2 provides an easy implement to measure signal frequency. The counter must be armed before the application of a desired signal. An armed counter will start counting on the first source edge after the Gate edge is asserted.. The counter will detect the voltage transaction twice and then automatically disarm itself. Measurement can be resumed by issuing a new ARM command.

Once a voltage transaction happens, the counter will generate TC and store the count value into registers. The first encountering voltage transaction will save the count value into Hold register and the second one will save the value into Load register. On the other words, the up cycle period and low cycle period are saved in Hold and Load registers respectively. Then the period, duty cycle and frequency of the desired signal can be easily obtained.




Mode L Waveforms

**Repetition:** Disable

**Reload Source:** Reload from LOAD or HOLD registers.

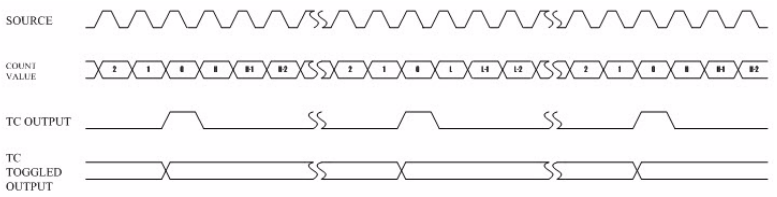
**Gate Mode:** Pulse Width Measurement

- **Mode J Waveform**
  **Variable Duty Cycle Rate Generator with No Hardware Gating**

  Mode J will find the greatest usage in frequency generation applications with variable duty cycle requirements. Once armed, the counter will count continuously until it is issued a DISARM command.

On the first TC, the counter will be reloaded from the **Hold** register. Counting will then proceed until the second TC at which time the counter will be reloaded from the **Load** register. Counting will continue, with the reload source alternating on each TC, until a DISARM command is issued to the counter. (The third TC reloads form the **Hold** register, the fourth TC reloads form the **Load** register, etc.)

Specifying the TC Toggled output in the Counter Mode register can generate a variable duty cycle output. The **Load** and **Hold** values then directly control the output duty cycle, with high resolution available when relatively high count values are used.




Mode M Waveforms

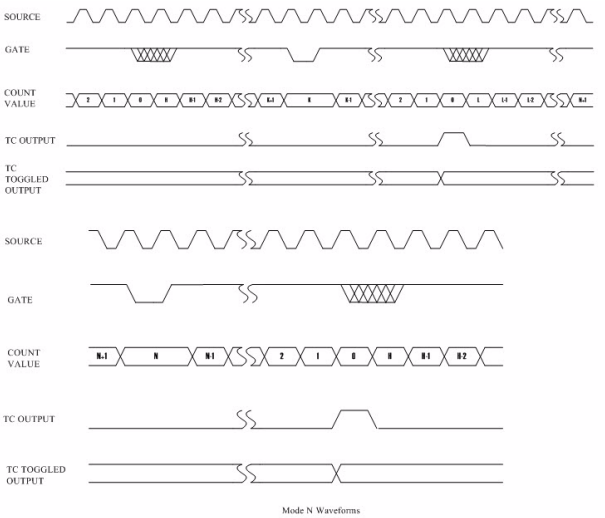
**Repetition:** Enable

**Reload Source:** Reload from LOAD or HOLD registers.

**Gate Mode:** No Gate control

- **Mode K Waveform**
  **Variable Duty Cycle Rate Generator with Level Gating**

  Mode K is identical to Mode J except that source edges are only counted when the Gate is active. The counter must be armed beforehand. Once armed, the counter will count all source edges that occur while the Gate is active and disregard those source edges that occur while the Gate is inactive. This permits the Gate to turn the count process on and off.
  As with Mode J, the reload source used will alternate on each TC, starting with the **Hold** register on the first TC after any allows the Gate to modulate the duty cycle of the output waveform. It can affect both the high and low portions of the output waveform.




Mode N Waveforms

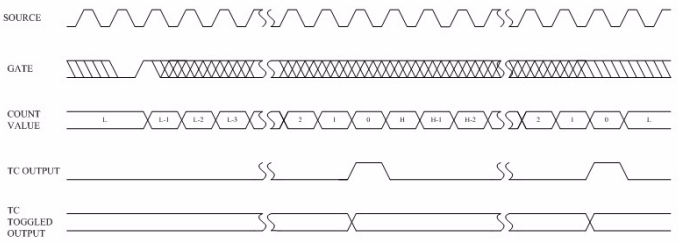
**Repetition:** Enable

**Reload Source:** Reload from LOAD or HOLD registers.

**Gate Mode:** Level Gate control

- **Mode L Waveform**
  **Hardware-Triggered Delayed Pulse One-Shot**

  Mode L is similar to Mode J except that counting will not begin until a Gate edge is applied to an armed counter. The counter must be armed before application of the triggering Gate edge; Gate edges applied to a disarmed counter are disregarded. The counter will start counting source edges and proceed until the second TC.
  Note that after application of a triggering Gate edge, the Gate input will be disregarded for the remainder of the count cycle. This differs from Mode N, where the gate can be modulated throughout the count cycle to stop and start the counter. On the first TC after application of the triggering Gate edge, the counter will be reloaded from the **Hold** register. On the second TC, the counter will be reloaded from the **Load** register and counting will stop until a new edge is issued to the counter. Note that unlike Mode K, new Gate edges are required alter every second TC to continue counting.




Mode O Waveforms

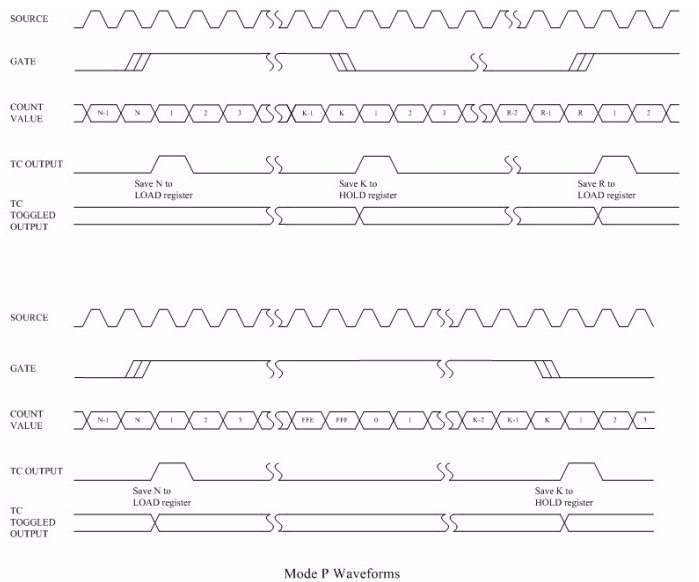
**Repetition:** Enable

**Reload Source:** Reload from LOAD or HOLD registers.

**Gate Mode:** Edge Gate control

- **Mode X3 Waveform**
  **Variable Duty Cycle/Frequency Monitoring**

  Mode X3 is similar to Mode X2 except that the counter will continuously monitor the variation of up cycle period and down cycle period until the reception of DISARM command. The data stored in **Hold** and **Load** registers are updated respectively when signal voltage transaction occurs. The counter must be armed before application of the triggering Gate edge. An armed counter will start counting on the first source edge after the triggering Gate edge. Countering will then proceed in the same manner as in Mode X2.




Mode P Waveforms

**Repetition:** Enable

**Reload Source:** Reload from LOAD or HOLD registers.

**Gate Mode:** Pulse Width Measurement